Tiziano Villa

Curriculum Vitae

Dipartimento di Informatica
Università degli Studi di Verona
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Interests

My research interests are in computer-aided design of electronic systems, with emphasis on logic synthesis and Boolean methods, on formal methods for the analysis and synthesis of cyberphysical systems, on automata theory and models of computation, on discrete event systems and supervisory control.

Education

Ph.D. in Electrical Engineering, May 1995
Department of Electrical Engineering and Computer Sciences (EECS)
University of California, Berkeley (UCB), USA

Master in Computer Sciences, May 1987
Department of Electrical Engineering and Computer Sciences (EECS), CS Division
University of California, Berkeley (UCB), USA

Mathematical Tripos Part III, Jun 1982
Department of Applied Mathematics and Theoretical Physics (DAMTP)
Cambridge University, United Kingdom

Diploma in Computational Mathematics, Feb 1978
University of Pisa, Italy

Batchelor in Mathematics, February 1977
State University of Milano, Milan, Italy

Positions

Full Professor, Oct 2006 - .
Department of Computer Science (DI)
University of Verona, Italy

Associate Professor, Nov 2002 - Sep 2006
Department of Electrical, Industrial and Mechanical Engineering (DIEGM)
University of Udine, Italy

Research Scientist, Feb 1997 - Oct 2002
PARADES Laboratories, Rome, Italy

Post-doctoral Researcher, Jun 1995 - Dec 1996
Electronics Research Laboratory (ERL)
University of California, Berkeley (UCB), USA

Research Assistant, Jan 1986 - May 1995
Electronics Research Laboratory (ERL)
University of California, Berkeley (UCB), USA

Research Engineer, Sep 1980 - Dec 1985
Integrated Circuits, Division of CSELT Laboratories, Turin, Italy

Software Engineer, March 1977 - Aug 1980
Italtel, Milan, Italy

Awards

Tong Leong Lim Pre-doctoral Prize, May 1991
Department of Electrical Engineering and Computer Science
University of California, Berkeley (USA)

Participation in National and International Research Projects

- OPERA 4.0 - Observation of business processes, with objective guarantees of privacy protection, for the prevention of errors and risk situations in an automatic manner at the time of Industry 4.0 (Research Project funded by Fondazione Cariverona, 1/4/2021-31/3/2023).

- Team Leader of the Project Computer Engineering for Industry 4.0 started January 2018. The National Evaluation Agency for research and university system (ANVUR) awarded the Department of Computer Science of the University of Verona a grant for being an Excellent Department. The project Computer Engineering for Industry 4.0 received funding for 8 million euro to be used in the next 5 years to extend the Department research areas with the development of a new research action in computer science for Industry 4.0, making the computer science technologies usable and accessible for companies in this new industrial reality (Research Project funded by MIUR, Italian Ministry of Education and Research, 2018-2022).

- Project leader of the project Metodi formali per la verifica e la sintesi di sistemi discreti e ibridi (Formal methods for the verification and synthesis of discrete and hybrid systems), INDAM, GNCS 2018 (Research project funded by MIUR, Italian Ministry of Education and Research, from Feb. 2018 to January 2019).

- TEMART - Tecnologie e materiali per la manifattura artistica i Beni Culturali l'arredo il decoro architettonico e urbano e il design del futuro (Technologies and materials for the applied arts and the restoration of the artistic heritage), July 2017 (Research project funded by Regione Veneto, from Nov. 2017 to October 2020).

- Team leader of the Verona unit and principal co-investigator of the workpackage WP10 *Tools for Design Automation*in the EU-funded project CON4COORD (alias C4C) FP7-ICT-2007.3.7(c) Grant Agreement nr. INFSO-ICT-228344, *Control for Coordination*, EU project coordinator Prof. Jan van Schuppen, CWI. The project was active from May 2008 to October

2011. The unit of Verona was in charge of the tasks related to tools for analysis and synthesis of distributed systems described by hybrid automata, formal methods for the verification of complex heterogeneous systems, networked distributed control.

- Scientific responsible of the project FSE 2007-2013 Asse Capitale Umano, 1695/1/4/2215/2009 *Tools for Synthesis of Discrete Controllers in Industrial Automation*, in partnership with an industrial company (EDALAB s.r.l., a local start-up in embedded systems design), sponsored jointly by the local government of Regione Veneto and the EU.

- Principal co-investigator of the Verona unit in the EU-funded project COCONUT FP7-2007-IST-1-217069, *A Correct-by-Construction Workbench for Design and Verification of Embedded Systems*, The project ran from January 2008 to June 2010. Responsible for the tasks *SAST: Tools for the verification and synthesis of hybrid and discrete automata* and *SEXTRACT: Extraction of temporal and functional constraints to compile hybrid automata into discrete representations preserving the properties verified in the hybrid domain.*

- Co-investigator of the project *Discrete Event System Optimization through Automata/FSM Equation Solving* funded by the NATO Collaborative Linkage Grant CBP.NR.CLG 982314. Project coordinator: Prof. R. Brayton, UC Berkeley, USA. The project ran from mid 2006 to mid 2008.

- Participant (PARADES unit) to the European Community Project IST2001-33520, entitled *Computation and Control*, project duration: 2002-2005.

- Principal co-investigator of the project *Logic synthesis and analysis through automata and language equation solving*, NATO Science Program, No. PST.CLG.979698, Collaborative Linkage Grant. No. 971217, project duration: 2003-2004.

- Participant (PARADES unit) to the CNR (National Research Council of Italy) Project in Applied Science, Madess II, sub-project 3.1.2, entitled *Design flow and architectures for engine control systems: models and methodologies*, duration: 1998-2001.

- Technical responsible of task *Automatic logic synthesis with PLAs*, European Community CVT project (CAD-VLSI for Telecommunications), project duration: 1983-1985.

- Recipient for year 1981 of an international scholarship of CNR, Mathematical Sciences Committee, to study computational mathematics for one year at DAMTP, Cambridge University, UK.

Professional Services

Tenure Committees for Foreign Universities

- Jury member of the committee to award the Habilitation à Diriger des Recherche to the candidate Natalia Kushik, Institut Polytechnique de Paris, September 2022 (Thèse de Habilitation à Diriger des Recherches: Contributions to Model Based Test Generation and Monitoring Strategies and their Networking Applications)

Editor

- Guest Editor of the special issue of Information and Computation *Formal Verification of Cyber-Physical Systems*, November 2022.
- Guest Editor of the special issue of Information and Computation *Fourth International Symposium on Games, Automata, Logics and Formal Verification (GandALF 2013)*, December 2015.
- Chief-Editor of the special issue of Proceedings of IEEE *Design Automation of Electronic systems: Past Accomplishments and Challenges Ahead*, November 2015.

Ph.D. Defense Committees

- Eduard Ionel Stan, Dottorato di Ricerca in Matematica - XXXV Ciclo, Universita' degli Studi di Parma, January 2023 (Foundations of Modal Symbolic Learning).
- Marco Esposito, Dottorato in Informatica - XXXIV Ciclo, Universita' di Roma La Sapienza, June 2022 (Simulation-Based Design Optimization of Critical Systems via Statistical Model Checking).
- Tommaso Masciulli, Dottorato di Ricerca in Information and Communication Technology - XXXIV Ciclo, Universita' degli Studi dell'Aquila, maggio 2022 (Control of Cyber-Physical Systems: a Formal Method Approach).
- Enrico Magnago, ICT International Doctoral School, Department of Information Engineering and Computer Science - Universita' degli Studi di Trento, april 2022 (Facing Infinity in Model Checking Expressive Specification Languages).
- Mirko Sessa, ICT International Doctoral School, Department of Information Engineering and Computer Science - Universita' degli Studi di Trento, ottobre 2019 (An SMT-based Framework for the Formal Analysis of Switched Multi-Domain Kirchhoff Networks).
- Lennart Swartjes, Technical University of Eindhoven, The Netherlands, September 2018 (Model-Based Design of Baggage-Handling Systems).
- Simone Silvetti, Universita' di Udine, September 2018 (Combining Machine Learning and Formal Methods for Complex Systems Design).
- Zahra Pooranian, Universita' di Roma La Sapienza, December 2016 (On Automating Design of Smart Grid Systems).
- Andrea Micheli, Universita' di Trento - Fondazione Bruno Kessler, January 2016 (Planning and Scheduling in Temporal Uncertain Domains).
- Vadim Alimguzhin, Universita' di Roma La Sapienza, December 2013 (Formal Model-Based Design of Control Software).
- Luigi Di Guglielmo, Universita' di Verona, 2012 (Refinement of Hybrid Automata: Code Generation and Verification).
- Christian Pilato, Politecnico di Milano, 2010 (Design Methodologies foe Embedded Systems with Hardware Accelerators).

- Mohammad Mostafizur Rahman Mozumdar, Politecnico di Torino, January 2010 (Modeling, Simulation, and Code Generation for Sensor Network Application Development).
- Vishal Sha, Politecnico di Torino, April 2008 (Synthesis of Dual-Rail Datapath Circuits).
- Davide Bañeres, Universitat Politecnica de Catalunya, Barcelona, February 2008 (Logic Synthesis Techniques for High-Speed Circuits).
- Alberto Casagrande, Universita' di Udine, March 2006 (Hybrid Systems: a First-Order Approach to Verification and Approximation Techniques).
- Ana Freitas, Instituto Superior Tecnico, Universidade Tecnica de Lisboa, Lisboa, 2002 (Power Estimation in Digital Circuits using Techniques of Implicit Enumeration: Estimacao de Potencia em Circuitos Utilizando Tecnicas de Enumeracao Implicita).
- Vasco Manquinho, Instituto Superior Tecnico, Universidade Tecnica de Lisboa, Lisboa, 1999 (Satisfiability-Based Pruning Techniques in Covering Algorithms).
- Robert Fuhrer, Columbia University, New York, 1999 (Sequential Optimization of Asynchronous and Synchronous Finite State Machines: Algorithms and Tools).

Services to the Technical Community

- Organizer and Co-Chair of the third Summer School on Formal Methods for Cyber-Physical Systems, Edition 2023: "Reactive Synthesis: Main Achievements and Current Trends", Udine, September 2023.
- Organizer and Co-Chair of the second Summer School on Formal Methods for Cyber-Physical Systems, Edition 2019: "Numerical and Symbolic Methods for Verification of Cyber-Physical Systems", Verona, June 2019.
- Organizer and Co-Chair of the first Summer School on Formal Methods for Cyber-Physical Systems, Edition 2017: "Automatic Synthesis of Controllers for Hybrid Systems", Verona, September 2017.
- Co-organized of the Workshop "Quo vadis, Logic Synthesis", co-located with DATE 2019, March 2019, Florence, Italy
- Organizer and Co-Chair of a special session on Emerging Technologies and Circuit Synthesis, for EUROMICRO DSD/SEAA 2015, 26-28 agosto 2015, Funchal, Madeira, Portugal.
- Organizer and Co-Chair of a special session on Emerging Technologies and Circuit Synthesis, for EUROMICRO DSD/SEAA 2014, 27-29 August 2014, Verona.
- Program Co-Chair of GandALF 2013, Fourth International Symposium on Games, Automata, Logics and Formal Verification, Borca di Cadore, Dolomiti, 29-31 August 2013.
- Organizer of a session on "Boolean Methods in Computer Science (MD-27)", "Stream: Boolean and Pseudo-Boolean Optimization", EURO XXVI (26th European Conference on Operational Research), 1-4 July 2013, Roma.

- Organizer of the Tutorial "A Design Automation of Electronic Systems: Past Accomplishments and Challenges Ahead - A Tribute to Robert Brayton", 18 March 2013, DATE 2013, Grenoble, France.
- Organizer of a session on "Boolean Methods in Computer Science", "Stream: Boolean and Pseudo-Boolean Optimization", EURO XXIV (24th European Conference on Operational Research), 11-14 July 2010, Lisbon, Portugal.
- Co-Chair of the Section "Work in Progress" of SIES 2010 (Symposium on Industrial Embedded Systems).
- Organizer of the Summer School 2009 of the UE Project C4C, Verona, 5-7 October 2009.
- Co-founder of GNSL (Giornata Nazionale di Sintesi Logica, Italian Annual Seminar Day on Logic Synthesis) and member of the steering and scientific committees from the beginning to now.
- Technical Program Committee of DATE (Design Automation and Test in Europe) from year 2001 to year 2024.
- Technical Program Committee of DAC (Design Automation Conference) for the years 2020 to 2023 (mentioning only the last years).
- Technical Program Committee of IWLS (International Workshop on Logic and Synthesis) from year 2002 to year 2023.
- Technical Program Committee of ICCAD (International Conference on Cimputer-Aided Design) and of ASP-DAC (Asian and South Pacific Conference on Computer-Aded Design) for various years.
- Technical Program Committee of MEMOCODE (International Symposium on Formal Methods and Models for System Design) for various years.
- Technical Program Committee of ADHS 2006, ADHS 2009 (IFAC Conference on Analysis and Design of Hybrid Systems).
- Technical Program and Organizing Committee of HSCC 2001 (Hybrid Systems: Computation and Control).
- Technical Program Committee of AICA 2005, track *Techniques for Verification and Specification of Complex Systems.*
- Frequent reviewer for Trans. Computer-Aided Design of ICs, Trans. Automatic Control, Trans. Computers, and many more archival journals.

Visits and Invited Talks

- Visiting scholar, CAD Group, Prof. Robert Brayton, EECS, UCB, summer yearly visits from years 2000 to 2018.
- Visiting scholar, Intel Strategic CAD Labs, Oregon, August 2000.

- Visiting industrial scholar, Cadence Berkeley Laboratory, Summer 1999.
- Visiting industrial scholar, Cadence Berkeley Laboratory, Summer 1998.
- Invited talks at the Università di Bologna, Università di Milano, Politecnico di Milano, Università di Parma, Università di Pisa, Università di Roma La Sapienza, Università di Udine, Università di Verona, University of California at Berkeley (USA), École Polutechnique Fèdèral de Lausanne (Switzerland), Technical University of Lisbon/INESC (Portugal), Polytechnical School of Saint Petersburg (RF), Tomsk State University (RF), Prague Charles University and Czech Technical University in Prague, Caesarea Rotschild Computer Science Institute/University of Haifa (Israel), DIMACS/RUTCOR at Rutgers University (USA).
- Invited Speaker at Conferences (only recent ones): PESW 2021 Prague Embedded Systems Week (Prague), APPSE 2019 VI International Conference on Actual Problems of System and Software Engineering, (Moscow, RF), ICAM 2018 XII Conference on Computer-Aided Technologies in Applied Mathematics (Gorno Altaisk, RF), ICTSS 2017 29th IFIP International Conference on Testing Software and Systems (St. Petersburg, RF), EPFL Workshop on Logic Synthesis and Verification 2015 (Lausanne, Switzerland).

Selected Publications

A list of selected publications is available from the author's institutional web address at the University of Verona http://www.di.univr.it/?ent=persona&id=3849&lang=en.

Books

- J. van Schuppen, T. Villa (eds.), *Coordination Control of Distributed Systems*, Springer Verlag, 2015
- Tiziano Villa, Nina Yevtushenko, Alan Mishchenko, Alexandre Petrenko, Alberto Sangiovanni Vincentelli, *The Unknown Component Problem: Theory and Applications*, Springer Verlag, 2012
- Tiziano Villa, Timothy Kam, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, *Synthesis of FSMs: Logic Optimization*, Kluwer/Springer Verlag, 1997, reprint 2012
- Timothy Kam, Tiziano Villa, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, *Synthesis of FSMs: Functional Optimization*, Kluwer/Springer Verlag, 1997, reprint 2010

Book Chapters

- Danila Gorodecky, Tiziano Villa, *Efficient Hardware Operations for the Residue Number System by Boolean Minimization,* in *Advanced Boolean Techniques,* R. Drechsler and M. Soeken eds., Springer, 2020 (**invited chapter**)
- Anna Bernasconi, Robert Brayton, Valentina Ciriani, Gabriella Trucco, and Tiziano Villa, *Synthesis of complemented circuits,* in *Further Improvements in the Boolean Domain,* Bernd Steinbach ed., Cambridge Scholars Publishing, 2018 (**invited chapter**)

- A. Bernasconi, V. Ciriani, G. Trucco, T. Villa, *Logic Synthesis by Signal-Driven Decomposition,* in *Advanced Techniques in Logic Synthesis, Optimizations and Applications,* K. Gulati and S.P. Khatri eds., Springer, 2010 (**invited chapter**)

- T. Villa, R. Brayton, A. Sangiovanni-Vincentelli, *Synthesis of Multi-Level Boolean Networks,* in *Boolean Models and Methods in Mathematics, Computer Science and Engineering,* Peter L. Hammer and Yves Crama eds., Encyclopedia of Mathematics and its Applications 134, Cambridge University Press, 2010 (**invited chapter**)

- J.-H. R. Jiang, T. Villa, *Hardware Equivalence and Property Verification,* in *Boolean Models and Methods in Mathematics, Computer Science and Engineering,* Peter L. Hammer and Yves Crama eds., Encyclopedia of Mathematics and its Applications 134, Cambridge University Press, 2010 (**invited chapter**)

- S. Hassoun, T. Villa, *Optimization of synchronous circuits,* in *Logic Synthesis and Verification,* T. Sasao and S. Hassoun eds., Kluwer Academic Publishers, 2002 (**invited chapter**)

- L. Lavagno, T. Villa, A. Sangiovanni-Vincentelli, *Advances in encoding for logic synthesis,* in *VLSI design environments,* G.W. Zobrist ed., Gordon and Breach Science Publishers, 2000 (**invited chapter**)

Peer-reviewed Articles in Journals and Conference Proceedings

1. Viktor Teren, Jordi Cortadella, Tiziano Villa, *Seto: a framework for the decomposition of Petri nets and transition systems,* Proceedings of the 26th Euromicro Conference on Digital System Design (DSD), Durres (Durazzo, Albania), September 2023

2. Viktor Teren, Jordi Cortadella, Tiziano Villa, *A framework for the decomposition of Petri nets and transition systems,* International Workshop on Logic & Synthesis (IWLS23), Lausanne, Switzerland, 2023

3. Luigi Capogrosso, Luca Geretti, Marco Cristani. Franco Fummi, Tiziano Villa, *Hermes-BDD: A Multi-Core and Multi-Platform Binary Decision Diagram Package,* 26th International Symposium on Design Diagnostics of Electronic Circuits and Systems DDECS 2023, Tallinn (Estonia), May 2023

4. V. Teren, J. Cortadella, T. Villa, *Generation of Synchronizing State Machines from a Transition System: a Region-based Approach,* International Journal of Applied Mathematics and Computer Science, Vol. 33, N. 1, 2023

5. Sanja Živanović, Pieter Collins, Luca Geretti, Davide Bresolin, Tiziano Villa, *A Higher Order Method for Input-Affine Uncertain Systems,* Nonlinear Analysis: Hybrid Systems, Vol. 47, February 2023, 101266

6. Matteo Zavatteri, Davide Bresolin, Romeo Rizzi, Tiziano Villa, *Dynamic Controllability of Temporal Networks via Supervisory Control,* Proceedings of Overlay 2022 (4th Workshop on Artificial Intelligence and fOrmal VERification, Logic, Automata, and sYnthesis), CEUR WORKSHOP PROCEEDINGS, Vol. 3311, Udine, 28 Nov. 2022

7. Luca Geretti, Pieter Collins, Davide Bresolin, Tiziano Villa, *Automating Numerical Parameters Along the Evolution of a Nonlinear System,* International Conference on Runtime Verification, Tbilisi, Georgia, 28-30 Sep. 2022, in Dang, T., Stolz, V. (eds) Runtime Verification. RV 2022. Lecture Notes in Computer Science, vol 13498. Springer, Cham

8. Luca Geretti, Alessandro Abate, Pierluigi Nuzzo, Tiziano Villa, *Editorial,* in *Information and Computation, Special Issue "Formal Verification of Cyber-Physical Systems", Vol. 289, November 2022, Article number 104979*

9. Matteo Zavatteri, Romeo Rizzi, Tiziano Villa, *Dynamic controllability of temporal networks with instantaneous reaction,* Information Sciences, Vol. 613, 2022

10. Viktor Teren, Jordi Cortadella, Tiziano Villa, *Decomposition of Transition Systems into Sets of Synchronizing Free-Choice Petri Nets,* Proceedings of the 25th Euromicro Conference on Digital System Design (DSD), Gran Canaria (Spain), September 2022

11. Viktor Teren, Jordi Cortadella, Tiziano Villa, *A Method of Transition System Decomposition into Sets of Synchronizing Free-Choice Petri Nets,* International Workshop on Logic & Synthesis (IWLS22), 2022

12. Luca Geretti, Stefano Centomo, Michele Boldo, Enrico Martini, Nicola Bombieri, Davide Quaglia, Tiziano Villa, *Process-driven Collision Prediction in Human-Robot Work Environments,* Proceedings of ETFA 2022, 27th International Conference on Emerging Technologies and Factory Automation, September 2022

13. Anna Bernasconi, Valentina Ciriani, Tiziano Villa, *Exploiting Symmetrization and D-reducibility for Approximate Logic Synthesis,* IEEE Transactions on Computers, Vol. 71, N. 1, January 2022

14. D. Bresolin, K. El-Faqih, T. Villa, N. Yevtushenko *Equivalence Checking and Intersection of Deterministic Timed Finite State Machines,* Formal Methods in System Design, Vol. 59, n. 4, 2021

15. Guido Sciavicco, Matteo Zavatteri, Tiziano Villa, *Mining CSTNUDs Significant for a Set of Traces is Polynomial,* Information and Computation, Volume 281, December 2021, 104773

16. Guido Sciavicco, Matteo Zavatteri, Tiziano Villa, *Mining Temporal Networks: Results and Open Problems,* Proceedings of Overlay@GandALF, September 2021

17. Viktor Teren, Jordi Cortadella, Tiziano Villa, *Decomposition of Transition Systems into Sets of Synchronizing State Machines,* Proceedings of the 24th Euromicro Conference on Digital System Design (DSD), Palermo, September 2021

18. Padmanabhan Balasubramanian, Anna Bernasconi, Valentina Ciriani, Tiziano Villa, *Boolean Heuristic for Disjoint SOP Synthesis,* Proceedings of the 24th Euromicro Conference on Digital System Design (DSD), Palermo, September 2021

19. Íñigo X. Íncer Romeo, Leonardo Mangeruca, Tiziano Villa, Alberto Sangiovanni-Vincentelli, *The Quotient in Preorder Theories,* GandALF 2020, Eleventh International Symposium on

Games, Automata, Logics and Formal Verification, J.-F. Raskin and D. Bresolin eds., EPTCS 326, September 2020

20. Davide Bresolin, Pieter Collins, Luca Geretti, Roberto Segala, Tiziano Villa, Sanja Živanović, *A Computable and Compositional Semantics for Hybrid Automata,* Proceedings of the 23rd ACM International Conference on Hybrid Systems: Computation and Control (HSCC 2020), Sidney, Australia, April 2020

21. A. Bernasconi, V. Ciriani, J. Cortadella, T. Villa, *Computing the Full Quotient in Bi-decomposition by Approximation,* Proceedings of DATE, Grenoble, France, March 2020

22. M. Zavatteri, R. Rizzi, T. Villa, *Dynamic Controllability and (J,K)-Resiliency of Generalized Constraint Networks with Uncertainty,* in Thirtieth Innternational Conference on Automatic Reasoning and Scheduling, ICAPS 2020, Nancy, France, October 2020

23. G. Sciavicco, M. Zavatteri, T. Villa, *Mining Significant Temporal Networks is Polynomial,* in 27th International Symposium on Temporal Representation and Reasoning, TIME 2020, Bolzano, Italy, October 2020

24. G. Sciavicco, M. Zavatteri, T. Villa, *Mining Significant Temporal Networks is Polynomial,* in 27th International Symposium on Temporal Representation and Reasoning, TIME 2020, Bolzano, Italy, October 2020

25. D. Bresolin, L. Geretti, T. Villa, *Automated Verification of Noisy Nonlinear Cyber-Physical Systems with Ariadne,* in Proceedings of OVERLAY 2019 Artificial Intelligence and Formal Verification, Logic, Automata, and Synthesis, Rende, Italy, November 2019

26. M. Zavatteri, R. Rizzi, T. Villa, *Strong Controllability of Temporal Networks with Decision,* in Proceedings of OVERLAY 2019 Artificial Intelligence and Formal Verification, Logic, Automata, and Synthesis, Rende, Italy, November 2019

27. M. Zavatteri, R. Rizzi, T. Villa, *Complexity of Weak, Strong and Dynamic Controllability of CNCUs,* in Proceedings of OVERLAY 2019 Artificial Intelligence and Formal Verification, Logic, Automata, and Synthesis, Rende, Italy, November 2019

28. I. Burdonov, A. Kossachev, N. Yevtushenko, T. Villa, *Synchronous Composition of Quasi-Complete and Quasi-Deterministic FSMs,* in Actual Problems of System and Software Engineering (APSSE 2019), VI International Conference, Moscow, Russia, November 2019

29. Luca Geretti, Sanja Živanović, Pieter Collins, Davide Bresolin, Tiziano Villa, *Rigorous continuous evolution of uncertain systems,* Proceedings of the 12th International Workshop on Numerical Software Verification, NSV 19, New York, USA, July 2019, in "Numerical Software Verification" (Majid Zamani and Damien Zufferey, eds.), LNCS 11652 and LNTCS 11652, Springer 2019

30. Danila Gorodecky, Tiziano Villa, *Efficient Implementation of Modular Division by Input Bit Splitting,* 26th IEEE Symposium on Computer Arithmetic, ARITH 26 (2019), Kyoto Research Park, Kyoto, Japan

31. A. Bernasconi, V. Ciriani, G. Trucco, T. Villa, *Boolean Minimization of Projected Sums of Products via Boolean Relations,* IEEE Transactions on Computers, Vol. 68, N. 9, September 2019

32. A. Bernasconi, V. Ciriani, T. Villa, *Approximate Logic Synthesis by Symmetrization,* Proceedings of DATE, Firenze, Italy, March 2019

33. Danila Gorodecky, Tiziano Villa, *Efficient Hardware Realization of Arithmetic Operations for the Residue Number System by Booelan Minimization,* 13th International Workshop on Boolean Problems, IWSBP 2018, Bremen, Germany, September 2018

34. André A. Geraldes, Luca Geretti, Davide Bresolin, Riccardo Muradore, Paolo Fiorini, Leonardo S. Mattos, Tiziano Villa, *Formal Verification of Medical CPS: a Laser Incision Case Study,* ACM Transactions on Cyber-Physical Systems, Vol. 2, N. 4, September 2018

35. D. Bresolin, A. Tvardovskii, N.Yevtushenko, T. Villa, M. Gromov *Minimizing Deterministic Timed Finite State Machines,* 14th IFAC Workshop on Discrete Event Systems WODES 2018, Sorrento, Italy, May-June 2018 (IFAC-PapersOnLine, Vol. 51, N. 7, 2018)

36. A. Bernasconi, V. Ciriani, L. Frontini, V. Liberali, G. Trucco, T. Villa, *Enhancing Logic Synthesis of Switching Lattices by Generalized Shannon Decomposition Methods,* Microprocessors and Microsystems: Embedded Hardware Design, Vol. 56, February 2018

37. Luca Geretti, Davide Bresolin, Pieter Collins, Sanja Živanovic, Tiziano Villa, *Ongoing work on automated verification of noisy nonlinear systems with Ariadne,* Proceedings of the 29th IFIP International Conference on Testing Software and Systems (ICTSS 2017), St.Petersburg, Russian Federation, October 2017, in "Testing Software and Systems" (N. Yevtushenko and A.R. Cavalli and H. Yenigün, eds.), LNCS 10533, Springer 2017

38. Luca Geretti, Riccardo Muradore, Davide Bresolin, Paolo Fiorini, Tiziano Villa, *Parametric Formal Verification: the Robotic Paint Spraying Case Study,* Proceedings of the 20th World Congress of the International Federation of Automatic Control, Toulouse, France, July 2017

39. Anna Bernasconi, Valentina Ciriani, Robert Brayton, Gabriella Trucco, and Tiziano Villa, *Complemented circuits,* 12th International Workshop on Boolean Problems, IWSBP 2016, Freiberg, Germany, September 2016

40. A. Bernasconi, V. Ciriani, L. Frontini, V. Liberali, G. Trucco, T. Villa, *Logic Synthesis for Switching Lattices by Decomposition with P-Circuits,* Proceedings of 19th EUROMICRO Conference on Digital System Design, DSD 2016, Limassol, Cyprus, August 2016

41. A. Bernasconi, V. Ciriani, G. Trucco, T. Villa, *Using Flexibility in P-Circuits by Boolean Relations,* IEEE Transactions on Computers, Vol. 64, N. 12, December 2015

42. R. Brayton, L. Carloni, A. Sangiovanni-Vincentelli, T. Villa, *Design Automation of Electronic Systems: Past Accomplishments and Challenges Ahead [Scanning the Issue],* Proceedings of IEEE, Vol. 103, N. 11, November 2015

43. T. Villa, A. Petrenko, N. Yevtushenko, A. Mishchenko, R. Brayton, *Component-Based Design by Solving Language Equations,* Proceedings of IEEE, Vol. 103, N. 11, November 2015

44. P. Nuzzo, A. Sangiovanni-Vincentelli, D. Bresolin, L. Geretti, T. Villa, *A Platform-Based Design Methodology with Contracts and Related Tools for the Design of Cyber-Physical Systems,* Proceedings of IEEE, Vol. 103, N. 11, November 2015

45. D. Bresolin, L. Geretti, R. Muradore, P. Fiorini, T. Villa, *Formal verification of robotic surgery tasks by reachability analysis,* Microprocessors and Microsystems: Embedded Hardware Design, Vol. 39, N. 8, November 2015

46. N. Yevtushenko, K. El-Faqih, T. Villa, Jie-Hong R. Jiang *Deriving Compositionally Deadlock-Free Components over Synchronous Automata Compositions,* The Computer Journal, Vol. 58, N. 11, November 2015

47. G. Castagnetti, M. Piccolo, T. Villa, N. Yevtushenko, R. Brayton, A. Mishchenko, *Automated Synthesis of Protocol Converters with BALM-II,* in *Software Engineering and Formal Methods, SEFM 2015 Collocated Workshops: ATSE, HOFM, MoKMaSD, and VERY*SCART, York, UK, September 7-8, 2015. Revised Selected Papers,* D. Bianculli and R. Calinescu and B. Rumpe eds., LNCS 9509, Springer, 2015 [presentato a VERY*SCART 2015: The Art of Service Composition and Formal Verification for Self-* Systems, co-located with SEFM 2015: 13th International Conference on Software Engineering and Fomal Methods, York, UK, September 2015]

48. A. Montanari, G. Puppis, T. Villa, *Editorial,* in *Information and Computation, Special Issue "Games, Automata, Logics, and Formal Verificatin (GandALF 2013)", Vol. 245, 1 December 2015*

49. A. Bernasconi, R. Brayton, V. Ciriani, G. Trucco, T. Villa, *Bi-decomposition using Boolean Relations,* Proceedings of 18th EUROMICRO Conference on Digital System Design, DSD 2015, Madeira, Portugal, August 2015

50. A. Bernasconi, R. Brayton, V. Ciriani, G. Trucco, T. Villa, *Minimization of Incompletely Specified Functions as Three-Level Logic via Boolean Relations,* nternational Workshop on Logic & Synthesis (IWLS15), 2015

51. E. Darusenkova, N. Yevtushenko, T. Villa, *Deriving a module of a multi agent system via Finite State Machine equation solving,* International Siberian Conference on Control and Communications, SIBCON-2015, Omsk, Russian Federation, May 2015

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Last updated: Monday 20$^{\text{th}}$ November, 2023