Nicola Bombieri

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Index

1 Short introduction

Nicola Bombieri is a Professor at the Department of Engineering for Innovation Medicine, University of Verona. His main research activity focuses on embedded software for cyber-physical systems, artificial intelligence at the edge, intelligent image and video analysis at the edge, heterogeneous architectures, Edge-Cloud computing, parallel computing, and parallel programming languages. He develops efficient software applications for multi-core, many-core, heterogeneous architectures targeting performance, power, and energy efficiency. His research field also includes electronic design automation (EDA), hardware description languages (HDLs), EDA applied to Systems Biology for network modeling and simulation. He served as Program Chair, Publication Chair, Technical Program Committee member, Workshops and Special Sessions Chair at ACM/IEEE conferences like DAC, DATE, ICCD, ICDH, HDPC, ICDH, MCSoC, SIES, ECSI FDL, CODES/ISSS, MEMOCODE, DSD, VLSI-SoC, ETS.

He has been involved in eight FP6/FP7/H2020 European Projects and several national MISE/FSE/Joint Projects/POR/RIRR with different roles, from principal investigator to project manager. He founded and is head of the *PARCO research lab* at the Department of Engineering for Innovation Medicine, University of Verona, which goal is the research and development of advanced programming techniques for cyber-physical systems and intelligent video analysis. He is author of more than 130 publications in international journals and conferences. He is Editor of two books.

2 Research activity

2.1 Summary

His main research activity focuses on embedded software for cyber-physical systems, artificial intelligence at the edge, intelligent image and video analysis at the edge, heterogeneous architectures, Edge-Cloud computing, parallel computing, and parallel programming languages. He develops efficient software applications for multi-core, many-core, heterogeneous architectures targeting performance, power, and energy efficiency. His research field also includes electronic design automation (EDA), hardware description languages (HDLs), EDA applied to Systems Biology for network modeling and simulation.

2.2 Organization, participation, management, and coordination of national and international research groups

- Nicola Bombieri began his research activity in 2005, by studying transaction level modeling (TLM) in the field of modeling and simulation of embedded systems under the supervision of Prof. Fummi at the Department of Computer Science, University of Verona and in collaboration with STMicroelectronics s.r.l., Milan, Italy. In 2006, he introduced the concept of *automatic abstraction* from register-transfer level (RTL) to TLM to accelerate system model simulation. The proposed automatic abstraction methodology has been implemented in a commercial tool and is currently one of the most referenced solutions for reusing existing RTL IPs into TLM systems via abstraction.
- He introduced the theory of event-based equivalence checking between RTL-TLM models at the University of Southampton (UK) in collaboration with Prof. Joao P. Marques-Silva in 2007. He proposed a methodology for RTL-TLM automatic transactor generation (which has been best paper candidate at ACM/IEEE DATE in 2008), the concept of mutation analysis applied to TLM verification (which has been best paper candidate at ACM/IEEE DATE in 2009), and the abstraction of SystemC data types for accelerating system simulation (which received the best paper award at ECSI/IEEE FDL in 2011).
- He worked on the reuse of RTL IPs through high-level synthesis at the Columbia University (NY), Computer Science Dept. in collaboration with Prof. L. Carloni in 2011 and 2012.
- He worked on parallel graph algorithms and data structures for dynamic sparse graphs in collaboration with David A. Bader (Georgia Tech, GA, USA).
- He worked on the parallel implementation of graph decomposition into strongly connected components (SCC problem) for GPUs in collaboration with M. Ceska (Oxford University, UK) and J. Barnat (Masaryk University, CZ).
- He worked on the parallel algorithms implementation for GPU targeting biological graph traversing in collaboration with Ivo Kwee (Institute of Oncology Research – IOR, Switzerland).
- He developed parallel implementations for searching off-target sites of Cas RNA-guided endonucleases for multi-core and many-core architectures in collaboration with Luca Pinello (Harvard Medical School – Massachusetts General Hospital Cancer Center, Boston, USA) and Daniel E. Bauer (Borad Insitute of MIT and Harvard). The results have been published in *Nature Genetics* in 2023.
- He worked on the parallelization of the sub-graph isomorphism algorithm and its implementation for multi-core architectures for Biological application in collaboration with D. Sasha (New York University, NY) and A. Ferro (University of Catania).
- He worked on bucket elimination problems for Artificial Intelligence applications and on embedded vision applications for autonomous driving in robotic applications in collaboration with A. Farinelli (University of Verona).
- He developed a performance model based on microbenchmarking for GPU applications in collaboration with F. Fummi (University of Verona). He applied GPU parallel computing in the field of embedded system design and verification, in collaboration with F. Fummi and G. Pravadelli (University of Verona).
- He worked on modeling and efficient simulation of biological systems through EDA methodologies and high-performance computing. In particular, he studied emerging properties through qualitative modeling of the intracellular signalling network controlling integrin activation

mediating leukocyte recruitment from the blood into the tissues, in collaboration with C. Laudanna (Department of Medicine, University of Verona).

- He has developed semi-qualitative modelling and efficient simulation of the purine metabolism to reproduce the metabolomics data obtained from naive lymphocytes and autoreactive T cells implicated in the induction of experimental autoimmune disorders with G. Constantin (Department of Medicine, University of Verona).
- He has applied his modeling and simulation framework for the robustness and sensitivity analysis of the Colitis-associated Colon Cancer (CAC) network and, more recently, for the analysis of the drug combinations that target the mitochondria in leukemia, in collaboration with G. Bader (Toronto University, CA).
- Since 2014, he has been working on design flows for rapid prototyping of heterogeneous software applications for cyber-physical systems and edge-Cloud computing. He studies methodologies to semi-automatically customize software for low-power, parallel, heterogeneous architectures considering multiple design constraints. He has developed techniques for model-based design of cyber-physical systems for Robotic and Industry 4.0 applications. He developed task mapping and scheduling approaches for embedded vision applications in collaboration with Prof. Hiren Patel, Univ. of Waterloo, Canada.
- Since 2018, he has been working on computer vision applications for parallel, heterogeneous (CPU/GPU), low-power architectures. In particular, he focused on real-time accurate 3D human pose estimation at the edge to enable motion analysis from videos and RGB/RGB-D sensors in the telemedicine practice. In collaboration with the group of Prof. Nicola Smania (Head of the Neurorehabilitation Ward of the Azienda Ospedaliera Universitaria Integrata di Verona (AOUI) and Director of the Neuromotor and Cognitive Rehabilitation Research Center at the Dept. Neuroscience, Biomedicine, and Movement Sciences – Univ. Verona), he designs advanced software for intelligent image and video analysis applied for clinical gait analysis.
- In collaboration with Prof. Michele Tinazzi (Head of Parkinson's center and Movement Disorders at the Dept. Neuroscience, Biomedicine, and Movement Sciences – Univ. Verona) he designs advanced software for intelligent image and video analysis for assessments of axial postural abnormalities in people with Parkinson's disease.

2.3 Research services

He serves as referee to several journals such as IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Embedded Computing Systems, ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on VLSI, IEEE Transactions on Computer-aided design of ICS, IEEE Design and Test of Computer, Elsevier Parallel Computing, IEEE Transactions on Computers and conferences such as ACM/IEEE DAC, ACM/IEEE DATE, IEEE/RSJ IROS, ACM/IEEE CODES, IEEE ICCAD, IEEE ETS, IEEE FDL, IEEE HLDVT, ACM/IEEE MEMOCODE, IEEE VLSI-SOC.

2.4 Organization of scientific meetings and conference committee participation

He serves/served as:

- Program Chair of IEEE International Conference on Edge Computing and Communications (EDGE), 2024.
- Topic Chair and Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2021. San Francisco, CA (USA), 5-9 December, 2021.
- DATE Executive Committee (DEC) member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2021. Grenoble (France), 1-5 Febrary, 2021.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2021. Grenoble (France), 1-5 Febrary, 2021.
- Technical Program Committee member of ACM International Symposium on High-Performance Parallel and Distributed Computing (HDPC), 2021, Stockholm (Sweden) 21-25 June, 2021.
- Publication Chair of IEEE/IFIP International Conference on Very Large Scale Integration (VLSI-

SOC), 4-8 October 2021, Singapore, Nanyang Technological University Center.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2020. San Francisco, CA (USA), 19-23 July, 2020.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2020. San Francisco, CA (USA), 19-23 July, 2020.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2020. Grenoble (France), 9-13 March, 2020.
- Technical Program Committee member of IEEE International Conference on Computer Design (ICCD) 2019. Abu Dhabi, UAE, 17-20 November 2019.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2019. Las Vegas, Nevada (USA), July, 2019.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2019. Florence (Italy), March, 2019.
- Technical Program Committee member of IEEE International Workshop on Advances in Parallel Programming Models and Frameworks for the Multi-/Many-core Era (APPMM in HPEC), 2019, Dublin, Ireland, 15-19 July 2019.
- Program Co-Chair of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2018. Verona (Italy), 8-10 October, 2018.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2018. San Francisco, CA (USA), 24-28 June, 2018.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2018. Dresden (Germany), 19-23 March, 2018.
- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2017. Abu Dhabi (UAE), 23-25 October, 2017.
- Technical Program Committee member of IEEE/ECSI Forum on Specification and Design Languages (FDL) 2017. Verona (Italy), 18-20 September 2017.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES) 2017. Toulouse (Frances), 14-16 June 2017.
- Keynote Chair, Special Session organizer, Special Session Chair at IEEE/ECSI Forum on specification and Design Languages (FDL) 2016, Bremen (Germany), 14-16 September 2016.
- Session Chair at IEEE International Symposium on Industrial Embedded Systems (SIES). Krakow (Poland), 23-25 May 2016.
- Technical Program Committee member of IEEE/ECSI Forum on Specification and Design Languages (FDL) 2016. Bremen (Germany), 14-16 September 2016
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES) 2016. Krakow (Poland), 23-25 May 2016.
- Workshops/Special Sessions Chair at IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC) 2015, Turin, Italy, 23-25 Sept. 2015.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES). Siegen (Germany), 8-10 June 2015.
- Hands-on tutorial co-organizer and speaker at ACM/IEEE Embedded Systems Week (CODES/ISSS) 2014. Title: Methods and tools for smart device integration and simulation. New Delhi – India. 12-17 Oct. 2014.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems – Work in Progress (SIES-WiP). Pisa (Italy), 18-20 June 2014.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES). Pisa (Italy), 18-20 June 2014.
- Technical Program Committee member of IEEE Euromicro Conference on Digital System Design (DSD) Cesme, Izmir- Turkey, 5-8 September 2012.
- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2011. Hong-Kong (China), 3-5 October, 2011.
- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2010. Madrid (Spain), 27-29 September 2010.

- Session Chair at ACM/IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2010. Grenoble (France), 26-28 June, 2010.
- Session Chair at IEEE European Test Symposium (ETS) 2009. Sevilla (Spain), 25-29 May, 2009.

2.5 European Project participations

He had technical and scientific participation in the following European Projects:

- ADAIR - From air pollution to brain pollution - novel biomarkers to unravel the link of air pollution and Alzheimer's disease – H2020 (2020-2023). Role: Responsible of activity related to high-performance computing.
- TOUCHMORE: Automatic Customizable Tool-chain for heterogeneous Multicore Platform Software Development (FP7-ICT-2011-7-288166). Starting date: 01/09/2011. Duration: 30 months. Role: Responsible of activity related to embedded software design and reconfiguration for the UNIVR partner.
- SMAC: Smart Systems Co-design (FP7-ICT-2011-7-288827). Starting date: 01/10/2011. Duration: 36 months. Role: Responsible of activity related to embedded software design for the UNIVR partner.
- COMPLEX: Codesign and Power Management in Platform-based Design-space Exploration (FP7-ICT-2009-4-247999). Duration 36 months. Role: Responsible of activity related to embedded software design for the UNIVR partner.
- COCONUT: A Correct-by-Construction Workbench for Design and Verification of Embedded Systems (FP7-2007-IST-1-217069). Starting date: 01/11/2008, Duration: 30 months. Role: Responsible of activity related to embedded software development for the UNIVR partner.
- VERTIGO: Verification and Validation of Embedded System Design workbench (FP6-2005-IST-5-033709). Starting date: 01/01/2006. Duration: 30 months. Role: research group member.
- CREDES: Centre of Research Excellence in Dependable Embedded Systems (FP7-REGPOT-2008-1). Starting date: 01/10/2009. Duration: 36 months. Role: research group member.

2.6 National project participations

- PREPARE: Personalized Engine for Prostate Cancer Evaluation (Ministero dello Sviluppo Economico – Accordi per l'innovazione). Starting date: 2023, duration: 36 months. > 420,000 euros raised funds. Role: Principal investigator and leader of the UNIVR partner.
- DYNAPP: Automated, dynamic, quantitative telemedicine assessment of Postural Abnormalities in Parkinson's disease through augmented human pose estimation software (Brain Research Foundation Verona ONLUS), 2022-2023. 24,000 euros raised funds. Role: Principal investigator.
- D-PAY: un sistema per il pagamento digitale automatico basato su intelligent video analitycs per esercizi pubblici con servizio al tavolo (Joint Research – Univ. Verona), 2022-2023. 60,000 euros raised funds. Role: Principal investigator.
- EDIPO: A computational solution for bringing neuroimaging genetic into translational research (CARIVERONA), 2020. Role: responsible of activity related to high-performance computing architecture.
- VIDIO: Una piattaforma per lo sviluppo di applicazioni di intelligenza artificiale basata su analisi intelligente di video per attività commerciali di ristorazione con servizio al tavolo (Joint Project 2019). Role: responsible of activity related to embedded vision applications development.
- Model-Based Design and Verication Flow for Embedded Vision Applications (InDAM 2019). Role: Principal investigator.
- DigitalRestaurant - una piattaforma per la gestione intelligente dei servizi di ristorazione (2019-2023). 70,000 euros raised funds. Role: Principal investigator.
- ROS-based design and synthesis of monitors for semi-formal verification of robotics applications. (InDAM 2020). Role: project manager of activity related to embedded SW for robotics applications.

- DSSNEST: Analisi e progettazione piattaforma per il supporto alle decisioni (DSS) ad alte prestazioni per la diagnosi di malattie oculari (NEST s.r.l. – UNIVR Joint Projects) 2018-2020. 50,000 euros raised funds. Role: Principal investigator.
- Progetto di eccellenza: Informatica per Industria 4.0 (ANVUR, 2018-2023). Role: responsible of edge computing applications, high-performance computer (HPC) architecture, containerization and orchestration for edge computing.
- GOTHEM: Global House Thermal & Electrical Energy Management (POR - Obiettivo "Incremento dell'attività di innovazione delle imprese" Parte FESR fondo europeo di sviluppo regionale 2014-2020). Role: responsible of embedded software design.
- PREDYCOS: Personalized REsponsive Dynamic COmplex System. (Project with Private entity NeoDataGroup http://www.neodatagroup.com, 2017) Duration 24 months, two research positions opened (12 months each), 110,000 euros raised founds. Role: responsible of embedded software design.
- High-performance computational models for biomedical information extraction and integration. (INDAM GNCS, 2017). Duration 12 months. Role: Project manager for HPC.
- Integrating national and international spontaneous adverse drug reaction knowledge bases for pattern discovery in pharmacovigilance. (INDAM GNCS, 2016). Duration 12 months. Role: responsible of software design.
- H2S: Framework per la generazione automatica di SW embedded tramite riuso di modelli RTL esistenti. (FSE Project, 2011). Duration 12 months. One research position opened (12 M), 24,000 euros raised founds. Role: Principal Investigator.
- OPTIMUM: OPTImizing dependability via MUtation analysis for Microelectronics (Joint Project di Ateneo, 2007). Starting date: 01/01/2011. Duration: 12 months. Role Technical Manager.
- EFFORT: Ambiente basato su EFSM per la progettazione e la verifica di software embedded (Joint Project di Ateneo, 2007). Starting date: 01/01/2008. Duration: 30 months. Role: Technical Manager.

2.7 Other research activities

He founded and is head of the *PARCO Lab* at the Department of Engineering for Innovation Medicine, University of Verona. The *PARCO Lab*, which goal is the research and development of advanced parallel programming techniques for CPU/GPU architectures, advanced software for cyber-physical systems, and edge computing for intelligent video analysis:

- Has been awarded as *GPU Research Center* from NVIDIA Corporation and funded with 2 Tesla K40 devices and 16 Jetson TK1,TX1, TX2, Nano embedded boards;
- Currently hosts 4 PhD students, 1 PostDoc, 1 research fellow, 3 Master students, and 14 intern students (for bachelor and master degree stage);
- Serves as multidisciplinary research laboratory for applying advanced software design techniques to:
  - Intelligent image/video analysis applied to human motion analysis for Neuroscience.
  - Graph traversal and analysis for Bioinformatics.
  - System design and simulation for Systems and Molecular Biology.
  - Cyber-physical systems design and verification for Robotics.

2.8 Academic and research experience at foreign institutions

He has been visiting researcher at

- New York University (NY), USA (Computer Science Department) from 20/May/2023 to 22/June/2023.
- Columbia University in the city of New York (NY), USA (Computer Science Department) from 01/August/2011 to 31/October/2011.
- Columbia University in the city of New York (NY), USA (Computer Science Department) from and from 15/May/2012 to 30/June/2012.
- University of Southampton - Electronics and Computer Science, UK from Sept/2006 to Feb/2007.

2.9 Grants, Awards, and selected invited talk

May 2023: Mobility grant from the University of Verona to join the Department of Computer Science – New York University as visiting scholar. Project title: "Parallel algorithm in GPU architectures for dynamic graphs analysis".

Sept 2021: Best paper candidate for the paper “A container-based design methodology for robotic applications on kubernetes edge-cloud architectures” (2021) Forum on Specification and Design Languages (FDL), Antibes, France.

July 2020: HiPEAC Paper Award 2020 to the paper “Late Breaking Results: Enabling Conteinerized Computing and Orchestration ofr ROS-based Robotic SW applications on Cloud-Server-Edge architectures” – S. Aldegheri, N. Bombieri, F. Fummi, S. Girardi, R. Muradore, N. Piccinelli presented at ACM/IEEE Design Automation Conference – San Francisco, California (USA), 2020.

Feb 2020: Invited talk at University of Florida, Dept. Computer and Information Science and Engineering “Virtual Coaching for Empowering Pre-Frail Elderly in Daily-Life Activity”.

Sept 2019: Best paper candidate for the paper “Efficient Simulation and Parametrization of Stochastic Petri Nets in SystemC: A Casa Study From Systems Biology” presented at IEEE Forum on Specification and Design Languages (FDL) 2019, Southampton, UK.

Feb 2019: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) for the project: “Model-based Design and Verification flow for Embedded Vision Applications”.

Sept 2017: HiPEAC Paper Award 2017 to the paper “Power-aware performance tuning of GPU applications through microbenchmarking” – N. Bombieri, F. Busato, F. Fummi presented at ACM/IEEE Design Automation Conference – Austin, Texas (USA), 2017.

July 2017: Innovation Award at IEEE/Amazon/DARPA Graph Challenge 2017. Oded Green, James Fox, Euna Kim, Federico Busato, Nicola Bombieri, Kartik Lakhotia, Shijie Zhou, Shreyas Singapura, Hanqing Zeng, Rajgopal Kannan, Viktor Prasanna, David A. Bader, "Quickly Finding a Truss in a Haystack".

Sept 2016: Talk at Italian Workshop on Embedded Systems (IWES) – Pisa. “An EDA Platform for Modeling and Simulation in Systems Biology”.

July 2016: Advanced course at GEVIS Visual Inspection Systems s.r.l. “Parallel programming for GPU architectures with OpenCL and OpenACC” (18 hours), Fidenza (PR), Italy.

June 2016: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) for the project “Integrating national and international spontaneous adverse drug reaction knowledge bases for pattern discovery in pharmacovigilance”.

June 2015: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) to participate to the ISMB/ECCB conference, 2015.

June 2014: Grant from Microsoft Corporation for the project “Italian MSDN Library content for Visual Studio 2013”.

May 2014: Advanced course at QR/Newtom s.r.l. “OpenCL and parallel programming for GPU architectures” (14 hours). Verona, Italy.

June 2013: Invited talk at Intel Corporation® - Hillsboro, Oregon – USA. “On the automatic abstraction of RTL IPs into SystemC TLM models.

February 2013: Invited talk at Embedded World Conference 2013. “Automatic HDL conversion and abstraction methodologies”. Nuremberg – Germany.

October 2012: Invited talk at STMicroelectronics s.r.l. – Catania- Italy. “A2T: Automatic abstraction of RTL IPs into TLM models”.

Sept. 2012: Grant from Microsoft Corporation for the project “Italian MSDN Translation Wiki 2012”.

February 2012: Cooperint grant from the University of Verona for joining the Department of Computer

Science - Columbia University in the City of New York as visiting scholar. Project title: "Advancements on improving design space of RTL IP logic synthesis through abstraction and high-level synthesis".

November 2011: Invited talk at ESA-European Space Agency-Italy (web seminar) “Accelerating RTL simulation through RTL-TLM abstraction”

September 2011: Best paper Award at IEEE/ECSI Forum for Design Languages (FDL)", Oldenburg, Germany,13-15 September, 2011, with the paper: N. Bombieri, F. Fummi, V. Guarnieri, F. Stefanni, S. Vinco,"Efficient Implementation and Abstraction of SystemC Data Types for Fast Simulation".

August 2011: Cooperint grant from the University of Verona for joining the Department of Computer Science - Columbia University in the City of New York as visiting scholar. Project title: "Improving design space of RTL IP logic synthesis through abstraction and high-level synthesis".

April 2011: Invited talk at Synopsys Inc. (web seminar) “Accelerating RTL simulation through RTL-TLM abstraction”

April 2009: Invited paper N. Bombieri, F. Fummi, G. Pravadelli, M. Hampton, F. Letombe, "Functional qualification of TLM verification" at ACM/IEEE Design, Automation and Test in Europe (DATE) , Nice, France , 20-24 April, 2009.

March 2008: Best paper candidate in the track “Verification & Low Power Design at ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, with the paper: N. Bombieri, F. Fummi, G. Pravadelli, "A Mutation Model for the SystemC TLM 2.0 Communication Interfaces".

March 2008: Best paper candidate in the track “Verification & Low Power Design at ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, with the paper: N. Bombieri, N. Deganello, F. Fummi, "Integrating RTL IPs into TLM Designs Through Automatic Transactor Generation".

June 2007: SIGDA grant for attending the PhD Forum at the ACM/IEEE Design Automation Conference (DAC’07) conference, San Diego, CA – USA.

June 2007: Invited talk at the “Third national conference of Logic Synthesis”, University of Verona, Italy.

June 2007: Invited talk at the Department of Electronic Engineering, University of Udine (Italy). Talk title “A TLM Design for Verification Methodology”.

May 2007: Second-place winner of the 3rd TTTC Doctoral Thesis Award Competition at the IEEE VLSI Test Symposium (VTS’07) conference, Berkeley, CA-USA.

April 2007: EDAA grant for attending the PhD Forum at the ACM/IEEE Design, Automation and Test in Europe (DATE’07) conference, Nice, France.

3 Publications

3.1 International Journals:

[J1] Lumpp, F., Panato, M., Bombieri, N., Fummi, F. "A design flow based on Docker and Kubernetes for ROS-based Robotic Software Applications". IEEE Transactions on Embedded Computing Systems, 2023, doi: doi.org/10.1145/3594539.

[J2] Artusi, C.A. and Geroin, C. and Imbalzano, G. and Camozzi, S. and Aldegheri, S. and Lopiano, L. and Tinazzi, M. and Bombieri, N. "Assessment of Axial Postural Abnormalities in Parkinsonism: Automatic Picture Analysis Software". Movement Disorders Clinical Practice, 2023, vol. 10(4), pp. 636-645, doi 10.1002/mdc3.13692.

[J3] Aldegheri, S. and Artusi, C.A. and Camozzi, S. and Di Marco, R. and Geroin, C. and Imbalzano, G. and Lopiano, L. and Tinazzi, M. and Bombieri, N. "Camera- and Viewpoint-Agnostic Evaluation of Axial Postural Abnormalities in People with Parkinson's Disease through Augmented Human Pose Estimation. Sensors, 2023, vol. 23(6), doi 10.3390/s23063193, n. 3193.

[J4] Cancellieri, S. and Zeng, J. and Lin, L.Y. and Tognon, M. and Nguyen, M.A. and Lin, J. and Bombieri, N. and Maitland, S.A. and Ciuculescu, M.-F. and Katta, V. and Tsai, S.Q. and Armant, M. and Wolfe, S.A. and Giugno, R. and Bauer, D.E. and Pinello, L. "Human genetic diversity alters off-target outcomes of therapeutic gene editing". Nature Genetics, 2023, vol. 55(1), pp. 34-43, doi 10.1038/s41588-022-01257-y.

[J5] Martini, E. and Boldo, M. and Aldegheri, S. and Valè, N. and Filippetti, M. and Smania, N. and Bertucco, M. and Picelli, A. and Bombieri, N. "Enabling Gait Analysis in the Telemedicine Practice through Portable and Accurate 3D Human Pose Estimation". Computer Methods and Programs in Biomedicine, 2022, vol. 225, doi 10.1016/j.cmpb.2022.107016, n. 107016.

[J6] Lumpp, F., Aldegheri, S., Patel, H.D., Bombieri, N. "Task Mapping and Scheduling for OpenVX Applications on Heterogeneous Multi/Many-Core Architectures"(2021) IEEE Transactions on Computers, 70 (8), art. no. 9354946, pp. 1148-1159.

[J7] Bombieri, N., Scaffeo, S., Mastrandrea, A., Caligola, S., Carlucci, T., Fummi, F., Laudanna, C., Constantin, G., Giugno, R. "SystemC Implementation of Stochastic Petri Nets for Simulation and Parameterization of Biological Networks"(2021) ACM Transactions on Embedded Computing Systems, 20 (4), art. no. 31.

[J8] De Marchi, M., Lumpp, F., Martini, E., Boldo, M., Aldegheri, S., Bombieri, N. "Efficient ros-compliant cpu-igpu communication on embedded platforms" (2021) Journal of Low Power Electronics and Applications, 11 (2), art. no. 24.

[J9] Mocci, J., Busato, F., Bombieri, N., Bonora, S., Muradore, R. "Efficient implementation of the Shack–Hartmann centroid extraction for edge computing" (2020) Journal of the Optical Society of America A: Optics and Image Science, and Vision, 37 (10), pp. 1548-1556.

[J10] S. Cancellieri, M.C. Canver, N. Bombieri, R. Giugno, L. Pinello. CRISPRitz: rapid, high-throughput, and variant-aware in silico off-target site identification for CRISPR genome editing. In Bioinformatics. 2020. Bioinformatics, 36(7) pp. 2001-2008- 2020.

[J11] N. Bombieri, F. Busato, A. Danese, L. Piccolboni, G. Pravadelli. "Mangrove: an Inference-based Dynamic Invariant Mining for GPU Architectures". In IEEE Transactions on Computers. Vol 69, issue 4, pp 606-620, 2020.

[J12] Vinco, S., Bombieri, N., Pagliari, D.J., Fummi, F., Macii, E., Poncino, M. "A cross-level verification methodology for digital IPs augmented with embedded timing monitors". In ACM Transactions on Design Automation of Electronic Systems, 24 (3), art. no. 27, 2019.

[J13] N. Bombieri, F. Busato, F. Fummi. "Pro++: A Profiling Framework for Primitive-based GPU Programming". In IEEE Transactions on Emerging Topics in Computing, vol. 6(3), 382-394. 2018. DOI: 10.1109-TETC-2016-2546554.

[J14] Busato, M., Distefano, R., Bates, F., Karim, K., Bossi, A.M., López Vilariño, J.M., Piletsky, S., Bombieri, N., Giorgetti, A. "MIRATE: MIps RATional dEsign Science Gateway". In Journal of integrative bioinformatics, 15 (4), 2018.

[J15] Bonnici, V., Busato, F., Aldegheri, S., Akhmedov, M., Cascione, L., Carmena, A.A., Bertoni, F., Bombieri, N., Kwee, I., Giugno, R. "cuRnet: An R package for graph traversing on GPU". In BMC Bioinformatics, 19, art. no. 356. 2018.

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