Nicola Bombieri

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1 Introduzione

Nicola Bombieri è Professore Ordinario presso il Dipartimento di Ingegneria per l'Innovazione Medicina, Università di Verona. La sua principale attività di ricerca si concentra su software embedded per sistemi cyber-fisici, intelligenza artificiale all'edge, analisi intelligente di immagini e video all'edge, architetture eterogenee, Edge-Cloud computing, calcolo parallelo e linguaggi di programmazione paralleli. Sviluppa applicazioni software efficienti per architetture multi-core, many-core ed eterogenee mirate a prestazioni, potenza ed efficienza energetica. Il suo campo di ricerca comprende anche l'automazione della progettazione elettronica (EDA), i linguaggi di descrizione dell'hardware (HDL), l'EDA applicato alla biologia dei sistemi per la modellazione e la simulazione di reti. Ha ricoperto il ruolo di presidente del programma, presidente delle pubblicazioni, membro del comitato del programma tecnico, presidente dei workshop e delle sessioni speciali alle conferenze ACM/IEEE come DAC, DATE, ICCD, ICDH, HDPC, ICDH, MCSoC, SIES, ECSI FDL, CODES/ISSS, MEMOCODE, DSD, VLSI-SoC, ETS.
È stato coinvolto in otto progetti europei FP6/FP7/H2020 e diversi progetti nazionali MISE/FSE/Joint Projects/POR/RIRR con diversi ruoli, dal ricercatore principale al project manager. Ha fondato ed è a capo del laboratorio di ricerca PARCO presso il Dipartimento di Ingegneria per l'Innovazione Medicina dell'Università di Verona, il cui obiettivo è la ricerca e lo sviluppo di tecniche avanzate di programmazione per sistemi cyber-fisici e analisi video intelligente. E' autore di oltre 130 pubblicazioni su riviste e convegni internazionali. È curatore di due libri.

2 Attività di ricerca

2.1 Sommario

La sua principale attività di ricerca si concentra su software embedded per sistemi cyber-fisici, intelligenza artificiale all'edge, analisi intelligente di immagini e video all'edge, architetture eterogenee, Edge-Cloud computing, calcolo parallelo e linguaggi di programmazione paralleli. Sviluppa applicazioni software efficienti per architetture multi-core, many-core ed eterogenee mirate a prestazioni, potenza ed efficienza energetica. Il suo campo di ricerca comprende anche l'automazione della progettazione elettronica (EDA), i linguaggi di descrizione dell'hardware (HDL), l'EDA applicato alla biologia dei sistemi per la modellazione e la simulazione di reti.

2.2 Organizzazione, partecipazione, gestione e coordinamento di gruppi di ricerca nazionali ed internazionali

- Nicola Bombieri inizia la sua attività di ricerca nel 2005, studiando Transaction Level Modeling (TLM) nel campo della modellazione e simulazione di sistemi embedded sotto la supervisione del Prof. Fummi presso il Dipartimento di Informatica dell'Università di Verona e in collaborazione con STMicroelectronics s.r.l., Milano, Italia. Nel 2006, ha introdotto il concetto di astrazione automatica dal livello di trasferimento dei registri (RTL) al TLM per accelerare la simulazione del modello di sistema. La metodologia di astrazione automatica proposta è stata implementata in uno strumento commerciale ed è attualmente una delle soluzioni più referenziate per riutilizzare gli IP RTL esistenti nei sistemi TLM tramite astrazione.
- Ha introdotto la teoria del controllo di equivalenza basato su eventi tra modelli RTL-TLM presso l'Università di Southampton (Regno Unito) in collaborazione con il Prof. Joao P. Marques-Silva nel 2007. Ha proposto una metodologia per la generazione automatica di transattori RTL-TLM (best paper candidate ad ACM/IEEE DATE nel 2008), il concetto di analisi delle mutazioni applicato alla verifica TLM (best paper candidate ad ACM/IEEE DATE nel 2009) e l'astrazione dei tipi di dati SystemC per l'accelerazione del sistema simulazione (che ha ricevuto il premio per il miglior articolo all'ECSI/IEEE FDL nel 2011).
- Ha lavorato sul riutilizzo di IP RTL attraverso sintesi di alto livello presso la Columbia University (NY), Dipartimento di Informatica in collaborazione con il Prof. L. Carloni nel 2011 e 2012.
- Ha lavorato su algoritmi di grafi paralleli e strutture dati per grafi sparsi dinamici in collaborazione con David A. Bader (Georgia Tech, GA, USA).
- Ha lavorato all'implementazione parallela della scomposizione di grafi in componenti fortemente connessi (problema SCC) per GPU in collaborazione con M. Ceska (Università di Oxford, UK) e J. Barnat (Università Masaryk, CZ).
- Ha lavorato all'implementazione di algoritmi paralleli per GPU mirati all'attraversamento di grafi biologici in collaborazione con Ivo Kwee (Istituto di ricerca oncologica – IOR, Svizzera).
- Ha sviluppato implementazioni parallele per la ricerca di siti off-target di endonucleasi guidate da Cas RNA per architetture multi-core e many-core in collaborazione con Luca Pinello (Harvard Medical School – Massachusetts General Hospital Cancer Center, Boston, USA) e Daniel E. Bauer (Borad Institute del MIT e Harvard). I risultati sono stati pubblicati su Nature Genetics nel 2023.
- Ha lavorato alla parallelizzazione dell'algoritmo di isomorfismo dei sottografi e alla sua implementazione per architetture multi-core per applicazioni biologiche in collaborazione con D. Sasha (New York University, NY) e A. Ferro (Università di Catania).
  Ha lavorato ad applicazioni di Intelligenza Artificiale e visione embedded per la guida autonoma in applicazioni robotiche in collaborazione con A. Farinelli (Università di Verona).
- Ha sviluppato un modello prestazionale basato sul microbenchmarking per applicazioni GPU in collaborazione con F. Fummi (Università di Verona). Ha applicato il calcolo parallelo GPU nel campo della progettazione e verifica di sistemi embedded, in collaborazione con F. Fummi e G. Pravadelli (Università di Verona).
- Ha lavorato sulla modellazione e simulazione efficiente di sistemi biologici attraverso metodologie EDA e calcolo ad alte prestazioni. In particolare, ha studiato proprietà emergenti attraverso la modellizzazione qualitativa della rete di segnalazione intracellulare che controlla

l'attivazione delle integrine che mediano il reclutamento dei leucociti dal sangue nei tessuti, in collaborazione con C. Laudanna (Dipartimento di Medicina, Università di Verona). Ha sviluppato modelli semi-qualitativi e simulazioni efficienti del metabolismo delle purine per riprodurre i dati metabolomici ottenuti da linfociti naive e cellule T autoreattive implicate nell'induzione di disordini autoimmuni sperimentali con G. Constantin (Dipartimento di Medicina, Università di Verona).

- Ha applicato il suo framework di modellizzazione e simulazione per l'analisi di robustezza e sensibilità della rete del cancro del colon associato alla colite (CAC) e, più recentemente, per l'analisi delle combinazioni di farmaci che colpiscono i mitocondri nella leucemia, in collaborazione con G. Bader (Università di Toronto, California).
- Dal 2014 si occupa di flussi di progettazione per la prototipazione rapida di applicazioni software eterogenee per sistemi cyber-fisici ed edge-Cloud computing. Studia metodologie per personalizzare in modo semiautomatico software per architetture a basso consumo, parallele ed eterogenee considerando molteplici vincoli di progettazione. Ha sviluppato tecniche per la progettazione model-based di sistemi cyber-fisici per applicazioni Robotiche e Industria 4.0. Ha sviluppato approcci di mappatura e pianificazione delle attività per applicazioni di visione integrata in collaborazione con il Prof. Hiren Patel, Univ. di Waterloo, Canada
- Dal 2018 lavora su applicazioni di computer vision per architetture parallele, eterogenee (CPU/GPU) e a basso consumo. In particolare, si è concentrato sulla stima accurata della posa umana 3D in tempo reale at the edge per consentire l'analisi del movimento da video e sensori RGB/RGB-D nella pratica della telemedicina. In collaborazione con il gruppo del Prof. Nicola Smania (Responsabile del Reparto di Neuroriabilitazione dell'Azienda Ospedaliera Universitaria Integrata di Verona (AOUI) e Direttore del Centro di Ricerca di Riabilitazione Neuromotoria e Cognitiva presso il Dip. Neuroscienze, Biomedicina e Movimento – Univ. . Verona), progetta software avanzati per l'analisi intelligente di immagini e video applicati all'analisi clinica del cammino.
- In collaborazione con il Prof. Michele Tinazzi (Responsabile del Centro Parkinson e Disturbi del Movimento presso il Dip. Neuroscienze, Biomedicina e Movimento – Univ. Verona) progetta software avanzati per l'analisi intelligente di immagini e video per la valutazione delle anomalie posturali assiali nelle persone con la malattia di Parkinson.

2.3 Servizi per la ricerca

È revisore di riviste quali IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Embedded Computing Systems, ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on VLSI, IEEE Transactions on Computer-aided design of ICS, IEEE Design e test di computer, Elsevier Parallel Computing, IEEE Transactions on Computers e conferenze come ACM/IEEE DAC, ACM/IEEE DATE, IEEE/RSJ IROS, ACM/IEEE CODES, IEEE ICCAD, IEEE ETS, IEEE FDL, IEEE HLDVT, ACM /MEMOCODE IEEE, IEEE VLSI-SOC.

2.4 Organizzazione di convegni scientifici e partecipazione a comitati congressuali

Ricopre/ha ricoperto I seguenti ruoli:

- Program Chair of IEEE International Conference on Edge Computing and Communications (EDGE), 2024.
- Topic Chair and Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2021. San Francisco, CA (USA), 5-9 December, 2021.
- DATE Executive Committee (DEC) member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2021. Grenoble (France), 1-5 Febrary, 2021.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2021. Grenoble (France), 1-5 Febrary, 2021.
- Technical Program Committee member of ACM International Symposium on High-Performance

Parallel and Distributed Computing (HDPC), 2021, Stockholm (Sweden) 21-25 June, 2021.
- Publication Chair of IEEE/IFIP International Conference on Very Large Scale Integration (VLSI-SOC), 4-8 October 2021, Singapore, Nanyang Technological University Center.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2020. San Francisco, CA (USA), 19-23 July, 2020.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2020. San Francisco, CA (USA), 19-23 July, 2020.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2020. Grenoble (France), 9-13 March, 2020.
- Technical Program Committee member of IEEE International Conference on Computer Design (ICCD) 2019. Abu Dhabi, UAE, 17-20 November 2019.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2019. Las Vegas, Nevada (USA), July, 2019.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2019. Florence (Italy), March, 2019.
- Technical Program Committee member of IEEE International Workshop on Advances in Parallel Programming Models and Frameworks for the Multi-/Many-core Era (APPMM in HPEC), 2019, Dublin, Ireland, 15-19 July 2019.
- Program Co-Chair of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2018. Verona (Italy), 8-10 October, 2018.
- Technical Program Committee member of ACM/IEEE Design Automation Conference (DAC), 2018. San Francisco, CA (USA), 24-28 June, 2018.
- Technical Program Committee member of ACM/IEEE Design, Automation and Test in Europe (DATE), 2018. Dresden (Germany), 19-23 March, 2018.
- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2017. Abu Dhabi (UAE), 23-25 October, 2017.
- Technical Program Committee member of IEEE/ECSI Forum on Specification and Design Languages (FDL) 2017. Verona (Italy), 18-20 September 2017.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES) 2017. Toulouse (Frances), 14-16 June 2017.
- Keynote Chair, Special Session organizer, Special Session Chair at IEEE/ECSI Forum on specification and Design Languages (FDL) 2016, Bremen (Germany), 14-16 September 2016.
- Session Chair at IEEE International Symposium on Industrial Embedded Systems (SIES). Krakow (Poland), 23-25 May 2016.
- Technical Program Committee member of IEEE/ECSI Forum on Specification and Design Languages (FDL) 2016. Bremen (Germany), 14-16 September 2016
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES) 2016. Krakow (Poland), 23-25 May 2016.
- Workshops/Special Sessions Chair at IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC) 2015, Turin, Italy, 23-25 Sept. 2015.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES). Siegen (Germany), 8-10 June 2015.
- Hands-on tutorial co-organizer and speaker at ACM/IEEE Embedded Systems Week (CODES/ISSS) 2014. Title: Methods and tools for smart device integration and simulation. New Delhi – India. 12-17 Oct. 2014.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems – Work in Progress (SIES-WiP). Pisa (Italy), 18-20 June 2014.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES). Pisa (Italy), 18-20 June 2014.
- Technical Program Committee member of IEEE Euromicro Conference on Digital System Design (DSD) Cesme, Izmir- Turkey, 5-8 September 2012.
- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2011. Hong-Kong (China), 3-5 October, 2011.

- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2010. Madrid (Spain), 27-29 September 2010.
- Session Chair at ACM/IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2010. Grenoble (France), 26-28 June, 2010.
- Session Chair at IEEE European Test Symposium (ETS) 2009. Sevilla (Spain), 25-29 May, 2009.

2.5 Partecipazione a progetti europei

Ha avuto partecipazioni tecnico-scientifiche ai seguenti Progetti Europei:

- ADAIR - From air pollution to brain pollution - novel biomarkers to unravel the link of air pollution and Alzheimer's disease – H2020 (2020-2023). Role: Responsible of activity related to high-performance computing.
- TOUCHMORE: Automatic Customizable Tool-chain for heterogeneous Multicore Platform Software Development (FP7-ICT-2011-7-288166). Starting date: 01/09/2011. Duration: 30 months. Role: Responsible of activity related to embedded software design and reconfiguration for the UNIVR partner.
- SMAC: Smart Systems Co-design (FP7-ICT-2011-7-288827). Starting date: 01/10/2011. Duration: 36 months. Role: Responsible of activity related to embedded software design for the UNIVR partner.
- COMPLEX: Codesign and Power Management in Platform-based Design-space Exploration (FP7-ICT-2009-4-247999). Duration 36 months. Role: Responsible of activity related to embedded software design for the UNIVR partner.
- COCONUT: A Correct-by-Construction Workbench for Design and Verification of Embedded Systems (FP7-2007-IST-1-217069). Starting date: 01/11/2008, Duration: 30 months. Role: Responsible of activity related to embedded software development for the UNIVR partner.
- VERTIGO: Verification and Validation of Embedded System Design workbench (FP6-2005-IST-5-033709). Starting date: 01/01/2006. Duration: 30 months. Role: research group member.
- CREDES: Centre of Research Excellence in Dependable Embedded Systems (FP7-REGPOT-2008-1). Starting date: 01/10/2009. Duration: 36 months. Role: research group member.

2.6 Partecipazione a progetti nazionali

- PREPARE: Personalized Engine for Prostate Cancer Evaluation (Ministero dello Sviluppo Economico – Accordi per l'innovazione). Starting date: 2023, duration: 36 months. > 420,000 euros raised funds. Role: Principal investigator and leader of the UNIVR partner.
- DYNAPP: Automated, dynamic, quantitative telemedicine assessment of Postural Abnormalities in Parkinson's disease through augmented human pose estimation software (Brain Research Foundation Verona ONLUS), 2022-2023. 24,000 euros raised funds. Role: Principal investigator.
- D-PAY: un sistema per il pagamento digitale automatico basato su intelligent video analitycs per esercizi pubblici con servizio al tavolo (Joint Research – Univ. Verona), 2022-2023. 60,000 euros raised funds. Role: Principal investigator.
- EDIPO: A computational solution for bringing neuroimaging genetic into translational research (CARIVERONA), 2020. Role: responsible of activity related to high-performance computing architecture.
- VIDIO: Una piattaforma per lo sviluppo di applicazioni di intelligenza artificiale basata su analisi intelligente di video per attività commerciali di ristorazione con servizio al tavolo (Joint Project 2019). Role: responsible of activity related to embedded vision applications development.
- Model-Based Design and Verication Flow for Embedded Vision Applications (InDAM 2019). Role: Principal investigator.
- DigitalRestaurant - una piattaforma per la gestione intelligente dei servizi di ristorazione (2019-2023). 70,000 euros raised funds. Role: Principal investigator.
- ROS-based design and synthesis of monitors for semi-formal verification of robotics applications. (InDAM 2020). Role: project manager of activity related to embedded SW for robotics applications.

- DSSNEST: Analisi e progettazione piattaforma per il supporto alle decisioni (DSS) ad alte prestazioni per la diagnosi di malattie oculari (NEST s.r.l. – UNIVR Joint Projects) 2018-2020. 50,000 euros raised funds. Role: Principal investigator.
- Progetto di eccellenza: Informatica per Industria 4.0 (ANVUR, 2018-2023). Role: responsible of edge computing applications, high-performance computer (HPC) architecture, containerization and orchestration for edge computing.
- GOTHEM: Global House Thermal & Electrical Energy Management (POR - Obiettivo "Incremento dell'attività di innovazione delle imprese" Parte FESR fondo europeo di sviluppo regionale 2014-2020). Role: responsible of embedded software design.
- PREDYCOS: Personalized REsponsive Dynamic COmplex System. (Project with Private entity NeoDataGroup http://www.neodatagroup.com, 2017) Duration 24 months, two research positions opened (12 months each), 110,000 euros raised founds. Role: responsible of embedded software design.
- High-performance computational models for biomedical information extraction and integration. (INDAM GNCS, 2017). Duration 12 months. Role: Project manager for HPC.
- Integrating national and international spontaneous adverse drug reaction knowledge bases for pattern discovery in pharmacovigilance. (INDAM GNCS, 2016). Duration 12 months. Role: responsible of software design.
- H2S: Framework per la generazione automatica di SW embedded tramite riuso di modelli RTL esistenti. (FSE Project, 2011). Duration 12 months. One research position opened (12 M), 24,000 euros raised founds. Role: Principal Investigator.
- OPTIMUM: OPTImizing dependability via MUtation analysis for Microelectronics (Joint Project di Ateneo, 2007). Starting date: 01/01/2011. Duration: 12 months. Role Technical Manager.
- EFFORT: Ambiente basato su EFSM per la progettazione e la verifica di software embedded (Joint Project di Ateneo, 2007). Starting date: 01/01/2008. Duration: 30 months. Role: Technical Manager.

2.7 Altre attività di ricerca

Ha fondato ed è responsabile del PARCO Lab presso il Dipartimento di Ingegneria per l'Innovazione Medicina, Università di Verona. Il PARCO Lab, che ha come obiettivo la ricerca e lo sviluppo di tecniche avanzate di programmazione parallela per architetture CPU/GPU, software avanzati per sistemi cyber-fisici ed edge computing per l'analisi video intelligente:

- È stato premiato come GPU Research Center da NVIDIA Corporation e finanziato con 2 dispositivi Tesla K40 e 16 schede integrate Jetson TK1,TX1, TX2, Nano;
- Attualmente ospita 4 dottorandi, 1 assegnista di ricerca, 1 assegnista di ricerca, 3 studenti di master e 14 studenti tirocinanti (per la laurea triennale e magistrale);
- Funge da laboratorio di ricerca multidisciplinare per l'applicazione di tecniche avanzate di progettazione software per:
    - Analisi intelligente di immagini/video applicata all'analisi del movimento umano per le neuroscienze.
    - Attraversamento e analisi di grafici per la Bioinformatica.
    - Progettazione e simulazione di sistemi per la biologia molecolare e dei sistemi.
    - Progettazione e verifica di sistemi cyber-fisici per la Robotica.

2.8 Esperienze accademiche e di ricerca presso istituzioni estere

È stato ricercatore in visita presso:

- New York University (NY), USA (Computer Science Department) from 20/May/2023 to 22/June/2023.
- Columbia University in the city of New York (NY), USA (Computer Science Department) from 01/August/2011 to 31/October/2011.
- Columbia University in the city of New York (NY), USA (Computer Science Department) from and from 15/May/2012 to 30/June/2012.

- University of Southampton - Electronics and Computer Science, UK from Sept/2006 to Feb/2007.

2.9 Premi, riconoscimenti e inviti come relatore a conferenza

May 2023: Mobility grant from the University of Verona to join the Department of Computer Science – New York University as visiting scholar. Project title: "Parallel algorithm in GPU architectures for dynamic graphs analysis".

Sept 2021: Best paper candidate for the paper "A container-based design methodology for robotic applications on kubernetes edge-cloud architectures" (2021) Forum on Specification and Design Languages (FDL), Antibes, France.

July 2020: HiPEAC Paper Award 2020 to the paper "Late Breaking Results: Enabling Conteinerized Computing and Orchestration ofr ROS-based Robotic SW applications on Cloud-Server-Edge architectures" – S. Aldegheri, N. Bombieri, F. Fummi, S. Girardi, R. Muradore, N. Piccinelli presented at ACM/IEEE Design Automation Conference – San Francisco, California (USA), 2020.

Feb 2020: Invited talk at University of Florida, Dept. Computer and Information Science and Engineering "Virtual Coaching for Empowering Pre-Frail Elderly in Daily-Life Activity".

Sept 2019: Best paper candidate for the paper "Efficient Simulation and Parametrization of Stochastic Petri Nets in SystemC: A Casa Study From Systems Biology" presented at IEEE Forum on Specification and Design Languages (FDL) 2019, Southampton, UK.

Feb 2019: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) for the project: "Model-based Design and Verification flow for Embedded Vision Applications".

Sept 2017: HiPEAC Paper Award 2017 to the paper "Power-aware performance tuning of GPU applications through microbenchmarking" – N. Bombieri, F. Busato, F. Fummi presented at ACM/IEEE Design Automation Conference – Austin, Texas (USA), 2017.

July 2017: Innovation Award at IEEE/Amazon/DARPA Graph Challenge 2017. Oded Green, James Fox, Euna Kim, Federico Busato, Nicola Bombieri, Kartik Lakhotia, Shijie Zhou, Shreyas Singapura, Hanqing Zeng, Rajgopal Kannan, Viktor Prasanna, David A. Bader, "Quickly Finding a Truss in a Haystack".

Sept 2016: Talk at Italian Workshop on Embedded Systems (IWES) – Pisa. "An EDA Platform for Modeling and Simulation in Systems Biology".

July 2016: Advanced course at GEVIS Visual Inspection Systems s.r.l. "Parallel programming for GPU architectures with OpenCL and OpenACC" (18 hours), Fidenza (PR), Italy.

June 2016: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) for the project "Integrating national and international spontaneous adverse drug reaction knowledge bases for pattern discovery in pharmacovigilance".

June 2015: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) to participate to the ISMB/ECCB conference, 2015.

June 2014: Grant from Microsoft Corporation for the project "Italian MSDN Library content for Visual Studio 2013".

May 2014: Advanced course at QR/Newtom s.r.l. "OpenCL and parallel programming for GPU architectures" (14 hours). Verona, Italy.

June 2013: Invited talk at Intel Corporation® - Hillsboro, Oregon – USA. "On the automatic abstraction of RTL IPs into SystemC TLM models.

February 2013: Invited talk at Embedded World Conference 2013. "Automatic HDL conversion and abstraction methodologies". Nuremberg – Germany.

October 2012: Invited talk at STMicroelectronics s.r.l. – Catania- Italy. "A2T: Automatic abstraction of RTL IPs into TLM models".

Sept. 2012: Grant from Microsoft Corporation for the project "Italian MSDN Translation Wiki 2012".

February 2012: Cooperint grant from the University of Verona for joining the Department of Computer Science - Columbia University in the City of New York as visiting scholar. Project title: "Advancements on improving design space of RTL IP logic synthesis through abstraction and high-level synthesis".

November 2011: Invited talk at ESA-European Space Agency-Italy (web seminar) “Accelerating RTL simulation through RTL-TLM abstraction”

September 2011: Best paper Award at IEEE/ECSI Forum for Design Languages (FDL)", Oldenburg, Germany,13-15 September, 2011, with the paper: N. Bombieri, F. Fummi, V. Guarnieri, F. Stefanni, S. Vinco,"Efficient Implementation and Abstraction of SystemC Data Types for Fast Simulation".

August 2011: Cooperint grant from the University of Verona for joining the Department of Computer Science - Columbia University in the City of New York as visiting scholar. Project title: "Improving design space of RTL IP logic synthesis through abstraction and high-level synthesis".

April 2011: Invited talk at Synopsys Inc. (web seminar) “Accelerating RTL simulation through RTL-TLM abstraction”

April 2009: Invited paper N. Bombieri, F. Fummi, G. Pravadelli, M. Hampton, F. Letombe, "Functional qualification of TLM verification" at ACM/IEEE Design, Automation and Test in Europe (DATE) , Nice, France , 20-24 April, 2009.

March 2008: Best paper candidate in the track “Verification & Low Power Design at ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, with the paper: N. Bombieri, F. Fummi, G. Pravadelli, "A Mutation Model for the SystemC TLM 2.0 Communication Interfaces".

March 2008: Best paper candidate in the track “Verification & Low Power Design at ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, with the paper: N. Bombieri, N. Deganello, F. Fummi, "Integrating RTL IPs into TLM Designs Through Automatic Transactor Generation".

June 2007: SIGDA grant for attending the PhD Forum at the ACM/IEEE Design Automation Conference (DAC’07) conference, San Diego, CA – USA.

June 2007: Invited talk at the “Third national conference of Logic Synthesis”, University of Verona, Italy.

June 2007: Invited talk at the Department of Electronic Engineering, University of Udine (Italy). Talk title “A TLM Design for Verification Methodology”.

May 2007: Second-place winner of the 3rd TTTC Doctoral Thesis Award Competition at the IEEE VLSI Test Symposium (VTS’07) conference, Berkeley, CA-USA.

April 2007: EDAA grant for attending the PhD Forum at the ACM/IEEE Design, Automation and Test in Europe (DATE’07) conference, Nice, France.

3 Pubblicazioni

3.1 International Journals:

[J1] Lumpp, F., Panato, M., Bombieri, N., Fummi, F. "A design flow based on Docker and Kubernetes for ROS-based Robotic Software Applications". IEEE Transactions on Embedded Computing Systems, 2023, doi: doi.org/10.1145/3594539.

[J2] Artusi, C.A. and Geroin, C. and Imbalzano, G. and Camozzi, S. and Aldegheri, S. and Lopiano, L. and Tinazzi, M. and Bombieri, N. "Assessment of Axial Postural Abnormalities in Parkinsonism: Automatic Picture Analysis Software". Movement Disorders Clinical Practice, 2023, vol. 10(4), pp. 636-645, doi 10.1002/mdc3.13692.

[J3] Aldegheri, S. and Artusi, C.A. and Camozzi, S. and Di Marco, R. and Geroin, C. and Imbalzano, G. and Lopiano, L. and Tinazzi, M. and Bombieri, N. "Camera- and Viewpoint-Agnostic Evaluation of Axial Postural Abnormalities in People with Parkinson's Disease through Augmented Human Pose Estimation. Sensors, 2023, vol. 23(6), doi 10.3390/s23063193, n. 3193.

[J4] Cancellieri, S. and Zeng, J. and Lin, L.Y. and Tognon, M. and Nguyen, M.A. and Lin, J. and Bombieri, N. and Maitland, S.A. and Ciuculescu, M.-F. and Katta, V. and Tsai, S.Q. and Armant, M. and Wolfe, S.A. and Giugno, R. and Bauer, D.E. and Pinello, L. "Human genetic diversity alters off-target outcomes of therapeutic gene editing". Nature Genetics, 2023, vol. 55(1), pp. 34-43, doi 10.1038/s41588-022-01257-y.

[J5] Martini, E. and Boldo, M. and Aldegheri, S. and Valè, N. and Filippetti, M. and Smania, N. and Bertucco, M. and Picelli, A. and Bombieri, N. "Enabling Gait Analysis in the Telemedicine Practice through Portable and Accurate 3D Human Pose Estimation". Computer Methods and Programs in Biomedicine, 2022, vol. 225, doi 10.1016/j.cmpb.2022.107016, n. 107016.

[J6] Lumpp, F., Aldegheri, S., Patel, H.D., Bombieri, N. "Task Mapping and Scheduling for OpenVX Applications on Heterogeneous Multi/Many-Core Architectures"(2021) IEEE Transactions on Computers, 70 (8), art. no. 9354946, pp. 1148-1159.

[J7] Bombieri, N., Scaffeo, S., Mastrandrea, A., Caligola, S., Carlucci, T., Fummi, F., Laudanna, C., Constantin, G., Giugno, R. "SystemC Implementation of Stochastic Petri Nets for Simulation and Parameterization of Biological Networks"(2021) ACM Transactions on Embedded Computing Systems, 20 (4), art. no. 31.

[J8] De Marchi, M., Lumpp, F., Martini, E., Boldo, M., Aldegheri, S., Bombieri, N. "Efficient ros-compliant cpu-igpu communication on embedded platforms" (2021) Journal of Low Power Electronics and Applications, 11 (2), art. no. 24.

[J9] Mocci, J., Busato, F., Bombieri, N., Bonora, S., Muradore, R. "Efficient implementation of the Shack–Hartmann centroid extraction for edge computing" (2020) Journal of the Optical Society of America A: Optics and Image Science, and Vision, 37 (10), pp. 1548-1556.

[J10] S. Cancellieri, M.C. Canver, N. Bombieri, R. Giugno, L. Pinello. CRISPRitz: rapid, high-throughput, and variant-aware in silico off-target site identification for CRISPR genome editing. In Bioinformatics. 2020. Bioinformatics, 36(7) pp. 2001-2008- 2020.

[J11] N. Bombieri, F. Busato, A. Danese, L. Piccolboni, G. Pravadelli. "Mangrove: an Inference-based Dynamic Invariant Mining for GPU Architectures". In IEEE Transactions on Computers. Vol 69, issue 4, pp 606-620, 2020.

[J12] Vinco, S., Bombieri, N., Pagliari, D.J., Fummi, F., Macii, E., Poncino, M. "A cross-level verification methodology for digital IPs augmented with embedded timing monitors". In ACM Transactions on Design Automation of Electronic Systems, 24 (3), art. no. 27, 2019.

[J13] N. Bombieri, F. Busato, F. Fummi. "Pro++: A Profiling Framework for Primitive-based GPU Programming". In IEEE Transactions on Emerging Topics in Computing, vol. 6(3), 382-394. 2018. DOI: 10.1109-TETC-2016-2546554.

[J14] Busato, M., Distefano, R., Bates, F., Karim, K., Bossi, A.M., López Vilariño, J.M., Piletsky, S., Bombieri, N., Giorgetti, A. "MIRATE: MIps RATional dEsign Science Gateway". In Journal of integrative bioinformatics, 15 (4), 2018.

[J15] Bonnici, V., Busato, F., Aldegheri, S., Akhmedov, M., Cascione, L., Carmena, A.A., Bertoni, F., Bombieri, N., Kwee, I., Giugno, R. "cuRnet: An R package for graph traversing on GPU". In BMC Bioinformatics, 19, art. no. 356. 2018.

[J16] Bonnici, V., De Caro, G., Constantino, G., Liuni, S., D'Elia, D., Bombieri, N., Licciulli, F., Giugno, R. “Arena-Idb: A platform to build human non-coding RNA interaction networks”. In BMC Bioinformatics, 19, art. no. 350, 2018.

[J17] F. Busato, N. Bombieri. “A dynamic approach for workload partitioning on GPU architectures”. In IEEE Transactions on Parallel and Distributed Systems, 2017, vol.28(6): 1535-1549. DOI: 10.1109/TPDS.2016.2631166.

[J18] F.Bistaffa, N. Bombieri, A. Farinelli. “An Efficient Approach for Accelerating Bucket Elimination on GPUs”. In IEEE Transactions on Cybernetics, 2017, vol.47(11): 3967-3979. DOI: 10.1109-TCYB.2016.2593773.

[J19] V. Bonnici, F. Busato, G. Micale, N. Bombieri, A. Pulvirenti, R. Giugno. “APPAGATO: an APproximate PArallel and stochastic GrAph querying TOol for biological networks”. Bioinformatics, 2016, vol.32(14):2159-66.

[J20] F. Busato, N. Bombieri. “An Efficient Implementation of the Bellman-Ford algorithm for Kepler GPU Architectures”. IEEE Transactions on Parallel and Distributed Systems, vol. 27, n.8, pp. 2222-2233, 2016.

[J21] N. Bombieri, D. Drogoudis, G. Gangemi, R. Gillon, M. Grosso, E. Macii, M. Poncino, S. Rinaudo. “Addressing the Smart Systems Design Challenge: The SMAC Platform”. Microprocessors and Microsystems. vol. 39, n.8, 2015, pp. 1158-1173.

[J22] N. Bombieri, F. Fummi, S. Vinco. “A Methodology to Recover RTL IP Functionality for Automatic Generation of SW Applications”. ACM Transactions on Design Automation of Electronic Systems. vol. 20 n.3, 2015, pp. 1-25, 2015.

[J23] F. Busato, N. Bombieri. “BFS-4K: an Efficient Implementation of BFS for Kepler GPU Architectures”. IEEE Transactions on Parallel and Distributed Systems. vol. 26, n.7, pp. 1826-1838, 2015.

[J24] N. Bombieri, F. Fummi, V. Guarnieri, G. Pravadelli, F. Stefanni, T. Ghasempouri, M. Lora, G. Auditore, M. Negro-Marcigaglia. “Reusing RTL assertion checkers for verification of SystemC TLM models”. Journal of Electronic Testing: Theory and Applications, vol. 31, n.2, 2015, pp. 167-80.

[J25] V. Bonnici, F. Russo, N. Bombieri, A. Pulvirenti, R. Giugno. “Comprehensive reconstruction and visualization of non-coding regulatory networks in human”. Frontiers in Bioengineering and Biotechnology. vol. 69, n. 2, 2014, pp. 1-22.

[J26] N. Bombieri; F. Fummi; V. Guarnieri, G. Pravadelli. “Testbench qualification of SystemC TLM protocols through Mutation Analysis”. IEEE Transactions on Computers. vol. 63, n. 5, 2014, pp. 1248-1261.

[J27] R. Giugno, V. Bonnici, N. Bombieri, A.Pulvirenti, A.Ferro, D. Shasha. “GRAPES: a Software for Parallel Searching on Biological Graphs targeting Multi-core Architectures” PLoS ONE, vol. 8, n. 10, 2013, pp. 1-17.

[J28] N. Bombieri, E.S.M. Ebeid, F. Fummi, M. Lora. “On the Reuse of Heterogeneous IPs into SysML Models for Integration Validation”. Journal of Electronic Testing: Theory and Applications. vol. 29, n.5, 2013, pp. 1-20

[J29] A. Acquaviva, N. Bombieri, F. Fummi, S. Vinco. “Semi-Automatic Generation of Device Drivers for Rapid Embedded Platform Development”. IEEE Transactions on CAD/ICAS. vol. 32, n. 9, 2013, pp. 1293-1306.

[J30] N. Bombieri, F. Fummi, V. Guarnieri. “FAST: An RTL Fault Simulation Framework based on RTL-to-TLM Abstraction”. Journal of Electronic Testing: Theory and Applications. vol. 28, n. 4, 2012, pp. 495-510.

[J31] N. Bombieri, F. Fummi, V. Guarnieri, F. Stefanni, S. Vinco. “HDTLib: an efficient implementation of SystemC data types for fast simulation at different abstraction levels”. International Journal on Design Automation for Embedded Systems, vol. 16(2), 2012, pp.115-135.

[J32] Guarnieri V. Di Guglielmo G., Bombieri N., Pravadelli G., Fummi, F, Hantson H., Raik J., Jenihhin M., Ubar R. “On the Reuse of TLM Mutation Analysis at RTL”. Journal of Electronic Testing: Theory and Applications, vol. 28, n. 4, 2012 , pp. 435-448.

[J33] N. Bombieri, F. Fummi, G. Pravadelli. “Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions”. IEEE Transactions on Computers. vol. 60, n. 12, 2011, pp. 1730-1743.

[J34] N. Bombieri, M. Ferrari, F. Fummi, G. Di Guglielmo, G. Pravadelli, F. Stefanni, A. Venturelli. "HIFSuite: Tools for HDL Code Conversion and Manipulation «EURASIP Journal on Embedded Systems. vol. 2010 , n. 436328 , 2010 , pp. 1-20.

[J35] N. Bombieri, F. Fummi, D. Quaglia. "System/Network Design Space Exploration based on TLM for Networked Embedded Systems" ACM Transactions on Embedded Computing Systems. vol. 9, n. 4, 2010, pp. 37:1-37:32.

[J36] N. Bombieri, F. Fummi, G. Pravadelli. "Reuse and Optimization of Testbenches and Properties in a TLM-to-RTL Design Flow". ACM Transactions on Design Automation of Electronic Systems. vol. 13, n. 3, 2008, pp. 47:1-47:22.

[J37] N. Bombieri, A. Fedeli, F. Fummi, G. Pravadelli. "Hybrid Incremental Assertion-Based Verification for Functional Validation in TLM Design Flows". IEEE Design &Test of Computers. vol. 24, n. 2, 2007, pp. 140-152.

3.2 International Conferences:

[C1] Lumpp, F., Fummi, F., Patel, H.D., Bombieri, N. "Containerization and Orchestration of Software for Autonomous Mobile Robots: a Case Study of Mixed-Criticality Tasks across Edge-Cloud Computing Platforms". (2022) IEEE International Conference on Intelligent Robots and Systems (IROS), 2022-October, pp. 9708-9713.

[C2] Boldo, M., Bombieri, N., Centomo, S., De Marchi, M., Demrozi, F., Pravadelli, G., Quaglia, D., Turetta, C. "Integrating Wearable and Camera Based Monitoring in the Digital Twin for Safety Assessment in the Industry 4.0 Era". (2022) Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 13704 LNCS, pp. 184-194.

[C3] Boldo, M., Bombieri, N., De Marchi, M., Geretti, L., Germiniani, S., Pravadelli, G. "Risk Assessment and Prediction in Human-Robot Interaction Through Assertion Mining and Pose Estimation". (2022) IEEE 23rd Latin American Test Symposium (LATS) 2022.

[C4] Geretti, L., Centomo, S., Boldo, M., Martini, E., Bombieri, N., Quaglia, D., Villa, T. "Process-driven Collision Prediction in Human-Robot Work Environments". (2022) IEEE International Conference on Emerging Technologies and Factory Automation, ETFA, 2022-September.

[C5] Martini, E., Boldo, M., Aldegheri, S., De Marchi, M., Vale, N., Filippetti, M., Smania, N., Bertucco, M., Picelli, A., Bombieri, N. "Real-time Human Pose Estimation at the Edge for Gait Analysis at a Distance" (2022) Proceedings – IEEE 18th Annual International Conference on Distributed Computing in Sensor Systems, DCOSS 2022, pp. 45-48.

[C6] Martini, E., Vale, N., Boldo, M., Righetti, A., Smania, N., Bombieri, N. "On the Pose Estimation Software for Measuring Movement Features in the Finger-to-Nose Test". (2022) Proceedings - 2022 IEEE International Conference on Digital Health, ICDH 2022, pp. 77-86.

[C7] Martini, E., Boldo, M., Aldegheri, S., Valè, N., Filippetti, M., Smania, N., Bertucco, M., Picelli, A., Bombieri, N. "Preserving Data Privacy and Accuracy of Human Pose Estimation Software Based on CNN s for Remote Gait Analysis". (2022) Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBS, 2022-July, pp. 3468-3471.

[C8] Lumpp, F., Patel, H.D., Bombieri, N. "A Framework for Optimizing CPU-iGPU Communication on Embedded Platforms"(2021) Proceedings - Design Automation Conference (DAC), 2021-December, pp. 685-690.

[C9] Lumpp, F., Panato, M., Fummi, F., Bombieri, N. "A container-based design methodology for robotic applications on kubernetes edge-cloud architectures" (2021) Forum on Specification and Design Languages (FDL), 2021-September, 8-10 September, Antibes, France.

[C10] Aldegheri, S., Bombieri, N., Germiniani, S., Moschin, F., Pravadelli, G. "A containerized ROS-compliant verification environment for robotic systems" (2021) Proceedings of Design, Automation and Test in Europe, DATE, 2021-February, art. no. 9474167, pp. 222-225.

[C11] Aldegheri, S., Bombieri, N., Fummi, F., Girardi, S., Muradore, R., Piccinelli, N. "Late breaking results: Enabling containerized computing and orchestration of ROS-based Robotic SW

applications on cloud-server-edge architectures" (2020) Proceedings - Design Automation Conference (DAC), 2020-July, art. no. 9218659.

[C12] Bombieri, N., Mastrandrea, A., Scaffeo, S., Caligola, S., Fummi, F., Laudanna, C., Constantin, G., Giugno, R. "On the simulation and automatic parametrization of metabolic networks through electronic design automation" (2020) Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 12313 LNBI, pp. 323-334.

[C13] S. Aldegheri, N. Bombieri, H.D. Patel. "On the Task Mapping and Scheduling for DAG-based Embedded Vision Applications on Heterogeneous Multi/Many-core Architectures". In Proc. of ACM/IEEE Design and Test in Europe (DATE). 9-13 March. 2020. Grenoble, France. Pp. 1-4.

[C14] V. Bonnici, R. Giugno, N. Bombieri. "An Efficient Implementation of a Subgraph Isomorphism Algorithm for GPUs". In Proc. of IEEE International Conference on Bioinformatics and Biomedicine (BIBM). 3-6 Dec. 2018. Madrid, Spain. Pp 1-8.

[C15] Caligola, S., Carlucci, T., Fummi, F., Laudanna, C., Constantin, G., Bombieri, N., Giugno, R. "Automatic Parameterization of the Purine Metabolism Pathway through Discrete Event-based Simulation". In Proc. of IEEE Conference on Computational Intelligence in Bioinformatics and Computational Biology (CIBCB). 9-11 July 2019. Certosa di Pontigliano, Siena, Italy. Pp. 1-11.

[C16] Bombieri, N., Bonnici, V., Giugno, R. "Parallel Searching on Biological Networks". In Proc. of IEEE Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP). 13-15 Feb. 2019, Pavia, Italy. Pp. 307-314.

[C17] F. Busato, N. Bombieri. "Configuring Graph Traversal Applications for GPUs: Analysis of Implementation Strategies and their Correlation with Graph Characteristics". In Proc. of IEEE International Conference on High Performance Computing & Simulation (HPCS). 15-19 July 2019. Dublin, Ireland. Pp. 1-7.

[C18] S. Aldegheri, N. Bombieri, D. BLoisi, A. Farinelli. "Data Flow ORB-SLAM for Real-time Performance on Embedded GPU Boards". In Proc. of IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS). 4-8 Nov. 2019. Macau, China. Pp1-6.

[C19] S. Caligola, T. Carlucci, F. Fummi, C. Laudanna, G. Constantin, N. Bombieri, R. Giugno. "Efficient Simulation and Parametrization of Stochastic Petri Nets in SystemC: A Case study from Systems Biology". In Proc. of IEEE Forum on specification & Design Languages (FDL). 2-4 Sept. 2019. Ireland, Dublin. Pp 1-7.

[C20] T. Ghasempuri, A. Danese, G. Pravadelli, N. Bombieri, J. Raik. "RTL assertion mining with automated RTLto-TLM abstraction". In Proc. of IEEE Forum on specification & Design Languages (FDL). 2-4 Sept. 2019 Southampton, UK. Pp. 1-8.

[C21] Aldegheri, S., Manzato, S., Bombieri, N. "Enhancing Performance of Computer Vision Applications on Low-Power Embedded Systems Through Heterogeneous Parallel Programming". In Proc. of IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC), 8-10 October, Verona (Italy), art. no. 8644937, pp. 119-124. 2018.

[C22] Aldegheri, S., Bombieri, N. "Rapid Prototyping of Embedded Vision Systems: Embedding Computer Vision Applications into Low-Power Heterogeneous Architectures". In Proc. of IEEE International Symposium on Rapid System Prototyping (RSP). 4-5 October, Turin (Italy) art. no. 8631995, pp. 63-69. 2018.

[C23] Bonnici, V., Giugno, R., Bombieri, N. "An Efficient Implementation of a Subgraph Isomorphism Algorithm for GPUs". In Proc. of IEEE International Conference on Bioinformatics and Biomedicine (BIBM), 3-6 December, Madrid, (Spain), art. no. 8621444, pp. 2674-2681. 2018.

[C24] Busato, F., Green, O., Bombieri, N., Bader, D.A. "Hornet: An Efficient Data Structure for Dynamic Sparse Graphs and Matrices on GPUs". In Proc. of IEEE High Performance Extreme Computing Conference (HPEC), 25-27 September, Waltham, MA, USA, art. no. 8547541, 2018.

[C25] Aldegheri, S., Bombieri, N., Dall'Ora, N., Fummi, F., Girardi, S., Panato, M. "A Framework for the Design and Simulation of Embedded Vision Applications Based on OpenVX and ROS". In Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), 27-30 May, art. no. 8351514, Florence, (Italy) 2018.

[C26] Busato, F., Bombieri, N. "Efficient Load Balancing Techniques for Graph Traversal Applications on GPUs". Lecture Notes in Computer Science (including subseries Lecture

Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 11014 LNCS, pp. 628-641. 2018.

[C27] Aldegheri, S., Bombieri, N. "Extending OpenVX for model-based design of embedded vision applications". In Proc. of IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC), 23-25 October, Abu Dhabi (UAE), art. no. 8203457, 2017.

[C28] F. Busato, N. Bombieri. "A performance, power, and energy efficiency analysis of load balancing techniques for GPUs". In Proc. of IEEE International Symposium on Industrial Embedded Systems (SIES) Toulouse, France 14 - 16 June 2017, pp. 1-8.

[C29] O. Green, J. Fox, E. Kim, F. Busato, N. Bombieri, K. Lakotia, S. Zhou, S.G. Singapura, H. Zeng, R. Kannan, V. K. Prasanna, D. A. Bader. "Quickly finding a truss in a haystack". In Proc. of EEE High Performance Extreme Computing Conference, HPEC 2017, Waltham, MA, USA, September 12-14, 2017, pp.1-7.

[C30] S. Aldegheri, D. D. Bloisi, J.J Blum, N. Bombieri, A. Farinelli. "Fast and Power-efficient Embedded Software Implementation of Digital Image Stabilization for Low-cost Autonomous Boats". In Proc. of Conference on Field and Service Robotics (FSR) Zurich, Switzerland September 12-15, 2017, pp. 1-14.

[C31] N. Bombieri, F. Busato, F. Fummi. "Power-aware Performance Tuning of GPU Applications Through Microbenchmarking". In Proc. of ACM/IEEE Design Automation Conference (DAC) Austin (TX), USA June 18-22, 2017, pp. 1-6.

[C32] L. Bottarelli, M. Bicego, J.J. Blum, N. Bombieri, A. Farinelli, L. Veggian. "Orienteering-based path selection for mobile sensors". In Proc. of 3rd Italian Workshop on Artificial Intelligence and Robotics, AIRO 2016; Genova; Italy; 28 November. Code 127707.

[C33] R. Distefano, N. Goncharenko, F.Fummi, R. Giugno, G. Bader, N. Bombieri. "SyQUAL: A platform for qualitative modelling and simulation of biological systems". In Proc. of IEEE International High-Level Design Validation and Test Workshop (HLDVT), Santa Cruz, CA-USA, October 7-8, 2016, pp.1-8.

[C34] N. Bombieri, F. Busato, F. Fummi, A Fine-grained Performance Model for GPU Architectures. In Proc. of ACM/IEEE Design, Automation and Test in Europe (DATE), Dresden, Germany, 14-18 March, 2016, pp.1-6.

[C35] D. Coati, R. Distefano, N. Bombieri, F. Fummi, M. Mirenda, C. Laudanna, R. Giugno, A SystemC-based Platform for Assertion-based Verification and Mutation Analysis in Systems Biology. In Proc. of IEEE Latin-American Test Symposium (LATS), Foz do Iguacu, Brazil, 6-8 April, 2016, pp. 1-6.

[C36] Bombieri, Nicola; Busato, Federico; Fummi, Franco; Scala, Michele: MIPP: A Microbenchmark Suite for Performance, Power, and Energy Consumption Characterization of GPU architectures. In Proc. of IEEE International Symposium on Industrial Embedded Systems. Krakow (Poland), 23-25 May 2016. pp 1-6.

[C37] S. Aldegheri, J. Barnat, N. Bombieri, F. Busato, M. Cˇeˇska, Milan. Parametric Multi-Step Scheme for GPU-Accelerated Graph Decomposition into Strongly Connected Components. In Proc. of EURO-Par PELGA 2016. Grenoblw (France) 22-26 August. Pp 1-12.

[C38] Bistaffa, Filippo; Bombieri, Nicola; Farinelli, Alessandro: CUBE: A CUDA approach for Bucket Elimination on GPUs. In Proc. of European Conference on Artificial Intelligence (ECAI). The Hague, Hollande, 29 Aug-2 Sept. 2016.

[C39] N. Bombieri, F. Busato; A. Danese; L. Piccolboni; G. Pravadelli, Exploiting GPU Architectures for Dynamic Invariant Mining. In Proceedings of "IEEE International Conference on Computer Design (ICCD)", New York City, NY- USA, October 18-21, 2015, pp. 1-4.

[C40] F. Busato, N. Bombieri. On the Load Balancing Techniques for GPU Applications Based on Prefix-scan. In Proceedings of "IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-15)", Turin, Italy, September, 23-25, 2015, pp. 1-8.

[C41] N. Bombieri, F. Busato, F.Fummi. An Enhanced Profiling Framework for the Analysis and Development of Parallel Primitives for GPUs. In Proceedings of "IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-15)", Turin, Italy, September, 23-25, 2015, pp. 1-8.

[C42] R. Distefano, F. Fummi, C. Laudanna, N. Bombieri, R. Giugno, A SystemC Platform for Signal Transduction Modelling and Simulation in Systems Biology. In Proceedings of "ACM Great lakes symposium on VLSI (GLSVLSI)", Pittsburgh, Pennsylvania, USA, May 20-22, 2015, pp. 1-4.

[C43] N. Bombieri, Riccardo Filippozzi, G. Pravadelli, F. Stefanni, RTL property abstraction for TLM assertion-based verification. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)" , Grenoble (France) , 9-13 March , 2015 , pp. 1-6.

[C44] V. Guarnieri, M. Petricca, A. Sassone, S. Vinco, N. Bombieri, F. Fummi, E. Macii, M. Poncino, A Cross-level Verification Methodology for Digital IPs Augmented with Embedded Timing Monitors. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Dresden, Germany, 24-28 March, 2014, pp. 1-6.

[C45] N. Bombieri, R. Distefano, G. Scardoni, F. Fummi, C. Laudanna, R. Giugno, Dynamic modeling and simulation of leukocyte integrin activation through an electronic design automation framework. In Proceedings of "Conference on Computational Methods in Systems Biology (CMSB)", Manchester, UK, 17-19 November, 2014 , pp. 1-12.

[C46] N. Bombieri, F. Fummi, V. Guarnieri, G. Pravadelli, F. Stefanni, T. Ghasempouri, M. Lora, G. Auditore, M. Negro-Marcigaglia, On the Reuse of RTL assertions in Systemc TLM Verification. In Proceedings of "IEEE Latin-American Test Workshop (LATW)", Fortaleza, Brasil, 12-15 March, 2014, pp. 1-6.

[C47] F. Bistaffa, A. Farinelli, N. Bombieri, Optimising Memory Management for Belief Propagation in Junction Trees using GPGPUs. In Proceedings of "IEEE International Conference on Parallel and Distributed Systems (ICPADS)", Hsinchu, Taiwan, 16-19 December, 2014, pp. 1-8.

[C48] N. Bombieri, H.-Y. Liu, F. Fummi, L. Carloni, A Method to Abstract RTL IP Blocks into C++ Code and Enable High-Level Synthesis. In Proceedings of "ACM/IEEE Design Automation Conference (DAC)", Austin, TX, USA, 2-6 June, 2013, pp. 1-9.

[C49] N. Bombieri, F. Fummi, S. Vinco, On the Automatic Generation of GPU-oriented Software Applications from RTL IPs. In Proceedings of "ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)", Montreal, Canada, Sept 29 - Oct 04, 2013, pp. 1-10.

[C50] N. Bombieri, E.S. Ebeid, F. Fummi, M. Lora, On the reuse of RTL IPs for SysML model generation. In Proceedings of "IEEE International Workshop on Microprocessor Test and Verification (MTV)", Austin, TX, USA, 10–12 December, 2013, pp. 54-59.

[C51] V. Bertacco, D. Chatterjee, N. Bombieri, F. Fummi, S. Vinco, A. M. Kaushik, H. D. Patel, On the Use of GP-GPUs for Accelerating Compute-intensive EDA Applications. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Grenoble, France, 18-22 March, 2013, pp. 1357-1366.

[C52] N. Bombieri, D. Forrini, F. Fummi, M. Laurenzi, S. Vinco, RTL IP abstraction into optimized embedded software. In Proceedings of "IEEE East-West Design & Test Symposium (EWDTS)", Rostov-on-Don (Russia), 27-30 Sept. 2013, 2013, pp. 1-5.

[C53] N. Bombieri, D. Drogoudis, G. Gangemi, R. Gillon, E. Macii, M. Poncino, S. Rinaudo, F. Stefanni, D. Trachanis, M. van Helvoort, SMAC: Smart Systems Co-Design. In Proceedings of "IEEE EUROMICRO DSD/SEAA", Santander, Spain, 4-6 September, 2013, pp. 1-7.

[C54] N. Bombieri, F. Fummi, V. Guarnieri, A. Acquaviva, Energy Aware TLM Platform Simulation via RTL Abstraction. In Proceedings of "IEEE International High Level Design Validation and Test Workshop (HLDVT)", Huntington Beach, CA, USA, 9-10 November, 2012, pp. 156-163.

[C55] N. Bombieri, F. Fummi, V. Guarnieri, FAST-GP: An RTL Functional Verification Framework based on Fault Simulation on GP-GPUs. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Dresden, Germany, 12-16 March, 2012, pp. 562-565.

[C56] D. Lorenz, K. Grüttner, N. Bombieri, V. Guarnieri, S. Bocchio, From RTL IP to functional system-level models with extra-functional properties. In Proceedings of "ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)", Tampere, Finland, 7-12 October, 2012, pp. 547-556.

[C57] A. Acquaviva, N. Bombieri, F. Fummi, S. Vinco, On the automatic synthesis of parallel SW from RTL models of hardware IPs. In Proceedings of "ACM Great lakes symposium on VLSI (GLSVLSI)", Salt Lake City, UT, USA, 3-4 May, 2012, pp. 71-74.

[C58] N. Bombieri, F. Fummi, V. Guarnieri, G. Pravadelli, S. Vinco, Redesign and Verification of RTL IPs through RTL-to-TLM Abstraction and TLM Synthesis. In Proceedings of "IEEE International Workshop on Microprocessor Test and Verification (MTV)", Austin, TX, USA, 10-12 December, 2012, pp. 76-81.

[C59] N. Bombieri, S. Vinco, V. Bertacco, D. Chatterje, SystemC simulation on GP-GPUs: CUDA vs. OpenCL in Proceedings of "ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES)", Tampere, Finland, 7-12 October 2012, pp. 343-352

[C60] N. Bombieri, F. Fummi, V. Guarnieri, Accelerating RTL Fault Simulation through RTL-to-TLM Abstraction. In Proceedings of "IEEE European Test Symposium (ETS)", Trondheim, Norway, 23-27 May, 2011, pp. 117-122.

[C61] N. Bombieri, F. Fummi, D. Quaglia, S. Vinco, Automatic interface generation for component reuse in HW-SW partitioning. In Proceedings of "IEEE EUROMICRO Conference on Digital System Design (DSD)", Oulu, Finland, August 31 - September 2, 2011, pp. 793-796.

[C62] N. Bombieri, F. Fummi, V. Guarnieri, F. Stefanni, S. Vinco, Efficient Implementation and Abstraction of SystemC Data Types for Fast Simulation. In Proceedings of "IEEE Forum for Design Languages (FDL)", Oldenburg, Germany, 13-15 September, 2011, pp. 142-148.

[C63] V. Guarnieri, N. Bombieri, G. Pravadelli, F. Fummi, H. Hantson, J. Raik, M. Jenihhin, R. Ubar, Mutation Analysis for SystemC Designs at TLM. In Proceedings of "IEEE Latin-American Test Workshop (LATW)", Porto de Galinhas (PE), Brazil, March, 27-30, 2011, pp. 1-6.

[C64] N. Bombieri, F. Fummi, G. Pravadelli, Abstraction of RTL IPs into Embedded Software. In ACM/IEEE Design Automation Conference (DAC), in Proceedings of "ACM/IEEE Design Automation Conference (DAC)", Anaheim, CA, USA, 13-18 June, 2010, pp. 24-29.

[C65] N. Bombieri, F. Fummi, V. Guarnieri, Automatic Synthesis of OSCI TLM-2.0 Models into RTL Bus-based IPs. In Proceedings of "IEEE International High Level Design Validation and Test Workshop (HLDVT)", Anaheim, CA, USA, 11-12 June, 2010, pp. 105-112.

[C66] N. Bombieri, G. Di Guglielmo, L. Di Guglielmo, M. Ferrari, F. Fummi, G. Pravadelli, F. Stefanni, A. Venturelli, HIFSuite: Tools for HDL Code Conversion and Manipulation. In Proceedings of "IEEE International High Level Design Validation and Test Workshop", Anaheim Convention Center, Anaheim, CA, June 11-12, 2010, pp. 40-41.

[C67] N. Bombieri, F. Fummi, V. Guarnieri, Model Checking on TLM-2.0 IPs through automatic TLM-to-RTL synthesis. In Proceedings of "IEEE International Conference on VLSI and System-on-Chip (VLSI-SoC)", Madrid, Spain, 27-29 September, 2010, pp. 61-66.

[C68] A. Acquaviva, N. Bombieri, F. Fummi, S. Vinco, Automatic Customization of Device Drivers for IP-cores Used with Assorted CPU Organizations. In Proceedings of "ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)", Grenoble, France, 11-16 October, 2009, pp. 173-182.

[C69] N. Bombieri, F. Fummi, G. Pravadelli, S. Vinco, Correct-by-construction generation of device drivers based on RTL testbenches. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Nice, France, 20-24 April, 2009, pp. 1500-1505.

[C70] N. Bombieri, F. Fummi, G. Pravadelli, M. Hampton, F. Letombe, Functional qualification of TLM verification. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Nice, France, 20-24 April, 2009, pp. 190-195.

[C71] N. Bombieri, F. Fummi, G. Pravadelli, On the Mutation Analysis of SystemC TLM-2.0 Standard. In Proceedings of "IEEE International Workshop on Microprocessor Test and Verification (MTV)", Austin, TX, USA, 7-9 December, 2009, pp. 32-37.

[C72] N. Bombieri, F. Fummi, G. Pravadelli, A Mutation Model for the SystemC TLM 2.0 Communication Interfaces. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, pp. 396-401.

[C73] N. Bombieri, N. Deganello, F. Fummi, Integrating RTL IPs into TLM Designs Through Automatic Transactor Generation. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, pp. 15-20.

[C74] N. Bombieri, F. Fummi, G. Pravadelli, RTL-TLM Equivalence Checking Based on Simulation. In Proceedings of "IEEE East-West Design & Test Symposium (EWDTS)", Lviv, Ukraine, October 9-13, 2008, pp. 214-217.

[C75] N. Bombieri, F. Fummi, Automatic Transactor Generation in TLM by Exploiting EFSMs. In Proceedings of "Design & Verification Conference & Exhibition (DVCon)", San Jose, CA, USA, 21-23 February, 2007, pp. 151-158.

[C76] N. Bombieri, F. Fummi, G. Pravadelli, Incremental ABV for Functional Validation of TL-to-RTL Design Refinement. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Acropolis, Nice, France, 16-20 April, 2007, pp. 882-887.

[C77] N. Bombieri, F. Fummi, J.P. Marques-Silva, G. Pravadelli, Towards Equivalence Checking Between TLM and RTL Models. In Proceedings of "ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)", Nice, France, 30 May - 1 June, 2007, pp. 113-122.

[C78] N. Bombieri, F. Fummi, G. Pravadelli, A Methodology for Abstracting RTL Designs into TL Descriptions. In Proceedings of "ACM/IEEE International Conference on Formal Methods and Models for Co-Design (MEMOCODE)", Napa Valley, CA, USA, 27-29 July, 2006, pp. 103-112.

[C79] N. Bombieri, F. Fummi, G. Pravadelli, A TLM Design for Verification Methodology in IEEE Ph.D. Research. In Proceedings of "IEEE Ph.D. Research in Microelectronics and Electronics (PRIME)", Otranto (LE), Italy, 12-15 June, 2006, pp. 337-340.

[C80] N. Bombieri, F. Fummi, G. Pravadelli, Incremental ABV for TL-to-RTL Design Refinement. In Proceedings of "IEEE East-West Design & Test International Workshop (EWDTW)", Sochi (Russia), September 15-19, 2006, pp. 100-107.

[C81] N. Bombieri, A. Fedeli, F. Fummi, On PSL Properties Re-use in SoC Design Flow Based on Transaction Level Modeling. In Proceedings of "IEEE International Workshop on Microprocessor Test and Verification (MTV)", Austin, TX, USA, 3-4 Nov. 2006, pp. 127-132.

[C82] N. Bombieri, F. Fummi, On the Automatic Transactor Generation in TLM-based Design Flows. In Proceedings of "IEEE International High Level Design Validation and Test Workshop (HLDVT)", Monterey, CA, USA, 8-10 November, 2006, pp. 85-92.

[C83] N. Bombieri, F. Fummi, G. Pravadelli, On the Evaluation of Transactor-based Verification for Reusing TLM Assertions and Testbenches at RTL. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 06-10 March, 2006, pp. 1-6.

[C84] N. Bombieri, F. Fummi, D. Quaglia, TLM/Network Design Space Exploration for Networked Embedded Systems. In Proceedings of "ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)", Seoul, Corea, 22-25 October, 2006, pp. 58-63.

[C85] N. Bombieri, F. Fummi, G. Pravadelli, Functional Verification of Networked Embedded Systems. In Proceedings of "ACM/IEEE International Symposium on Quality Electronic Design (ISQED)", San Jose, CA, USA, 21-23 March, 2005, pp. 321-326.

[C86] N. Bombieri, A. Fedeli, F. Fummi, On the Property-based Verification in SoC Design Flow Founded on Transaction Level Modeling. In Proceedings of "ACM/IEEE International Conference on Formal Methods and Models for Codesigns (MEMOCODE)", Verona, Italy, 11-14 July, 2005, pp. 239-240.

[C87] N. Bombieri, F. Fummi, G. Pravadelli, At-Speed Functional Verification of Programmable Devices. In Proceedings of "IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)", Cannes, France, 11-13 October, 2004, pp. 386-394.

3.3 Libri:

[B1] N. Bombieri, G. Pravadelli, M. Fujita, T. Austin, R. Reis. “VLSI-SoC Design and Engineering of Electronics Systems Based on New Computing Paradigms”. IFIP/IEEE Advances in Information and Communication Technology. Vo. 561, ISBN: 978-303023424-9, Springer, 2019.

[B2] N. Bombieri, M. Poncino, G. Pravadelli. Smart Systems Integration and Simulation. Springer International Publishing. 2016. ISBN: 978-3-319-27390-7.

3.4 Capitoli di libro

[BC1] S. Aldegheri, N. Bombieri. “Integrating Simulink, OpenVX, and ROS for Model-Based Design of Embedded Vision Applications”. IFIP Advances in Information and Communication Technology, 500, pp. 178-197. Springer-Nature.2019

[BC2] F. Busato, N. Bombieri. “Graph Algorithms on GPUs” in Advances in GPU Research and Practice. Ed. H. Sarbazi Azad. Elsevier inc. In printing, Jan. 2017. ISBN: 978-0-12-803738-6.
[BC3] N. Bombieri, F.Fummi, G.Pravadelli “Hardware Design and Simulation for Verification” in M. Bernardo, A. Cimatti – Formal Methods for Hardware Verification. Springer, 2006, Pp. 1--29.

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